

Presented at the 15th Vienna Conference on Instrumentation (VCI), 18-22 February 2019

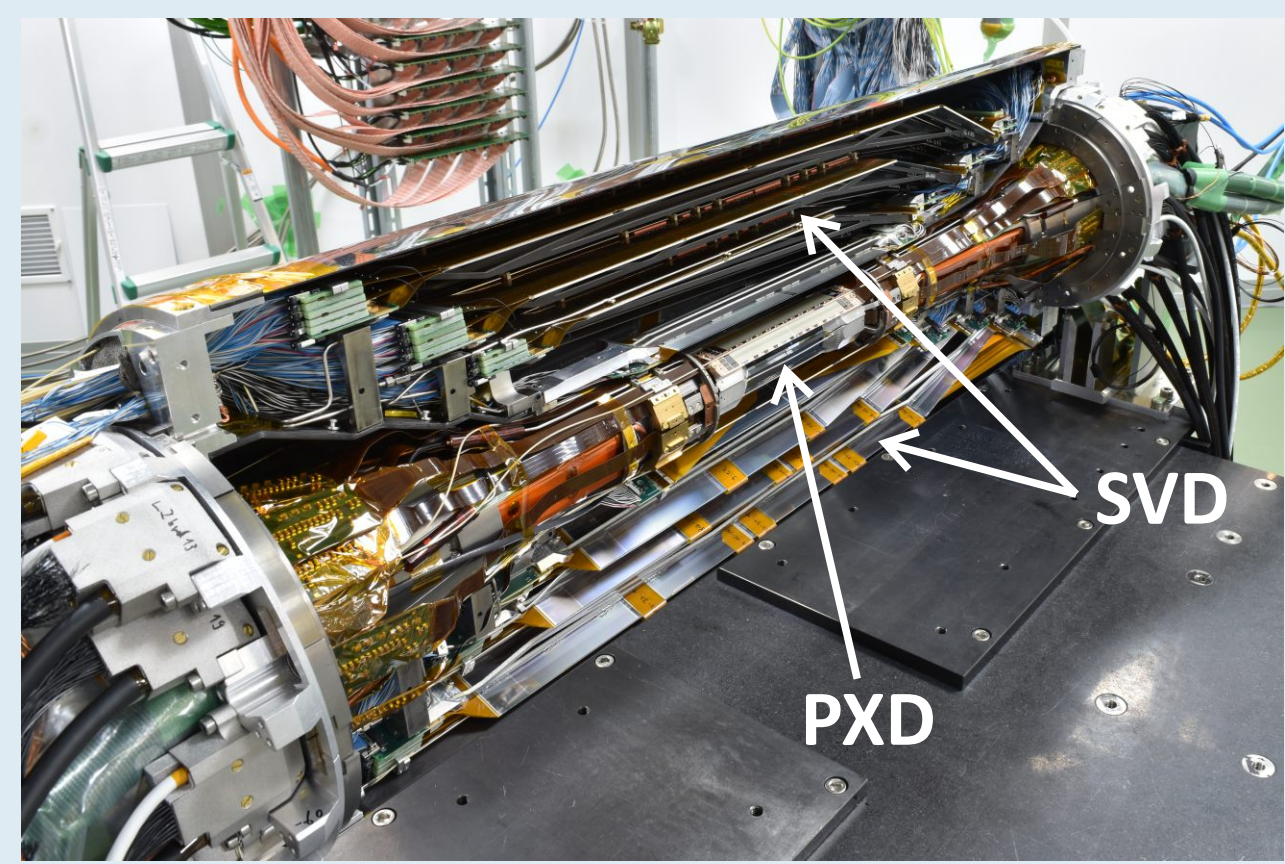
C. Irmeler\*, H. Yin on behalf of the Belle II SVD group

**ABSTRACT**  
The Belle II Silicon Vertex Detector (SVD) has been installed recently and is now prepared for physics run at SuperKEKB factory, Tsukuba, Japan. For a reliable operation and data taking of the SVD a sophisticated and robust run and slow control system has been implemented, which utilizes the Experimental Physics and Industrial Control System (EPICS) framework. EPICS uses client/server and publish/subscribe techniques to communicate

between the various sub-systems and computers. The information exchange between the different pieces of software and computers is done by process variables (PVs). These PVs are provided by input/output controllers (IOCs), which communicate and interface with the hardware components. The Belle II SVD slow and run control comprises of five groups of subsystems, which are SVD DAQ controller, Flash ADC controller, environmental monitors and

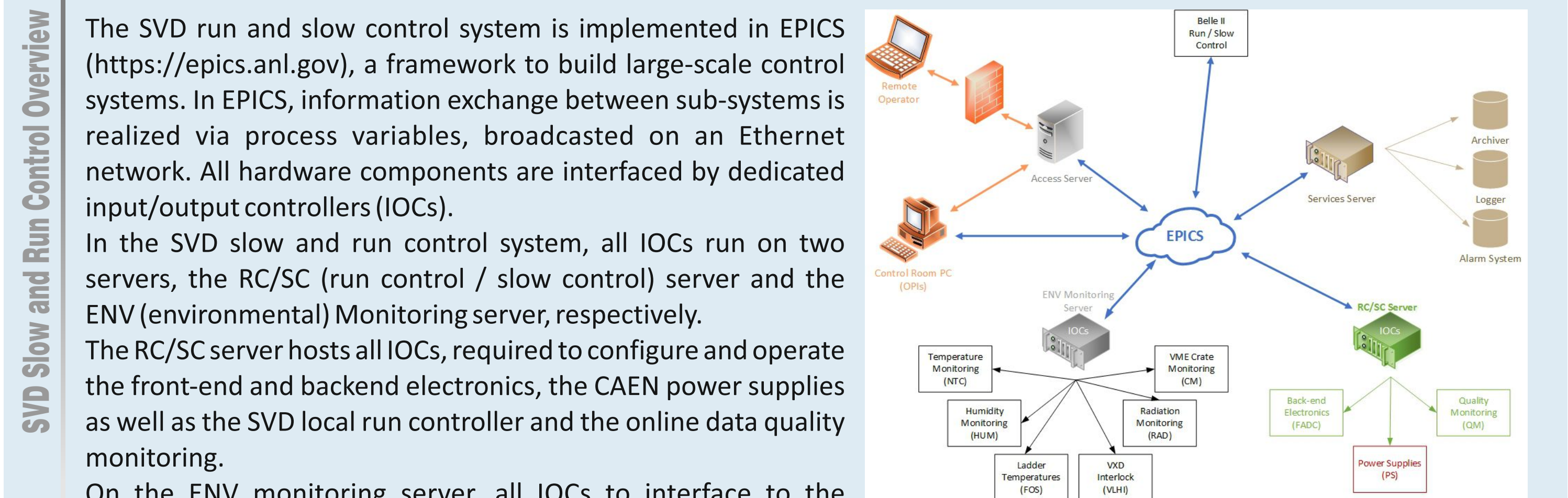
interlocks, power supplies and EPICS infrastructure services. In this presentation we describe tasks and implementation of the individual sub-systems, the interaction between them and the global Belle II run and slow control as well as first experiences from commissioning and initial operation of the SuperKEKB accelerator.

**BELLE II Silicon Vertex Detector**  
The Belle II silicon vertex detector (SVD) is the outer sub-system of the Belle II vertex detector (VXD). It is made from 4 layers of double-sided silicon strip detectors (DSSD), embracing the 2 layers of DEPFET pixel detectors (PXD).



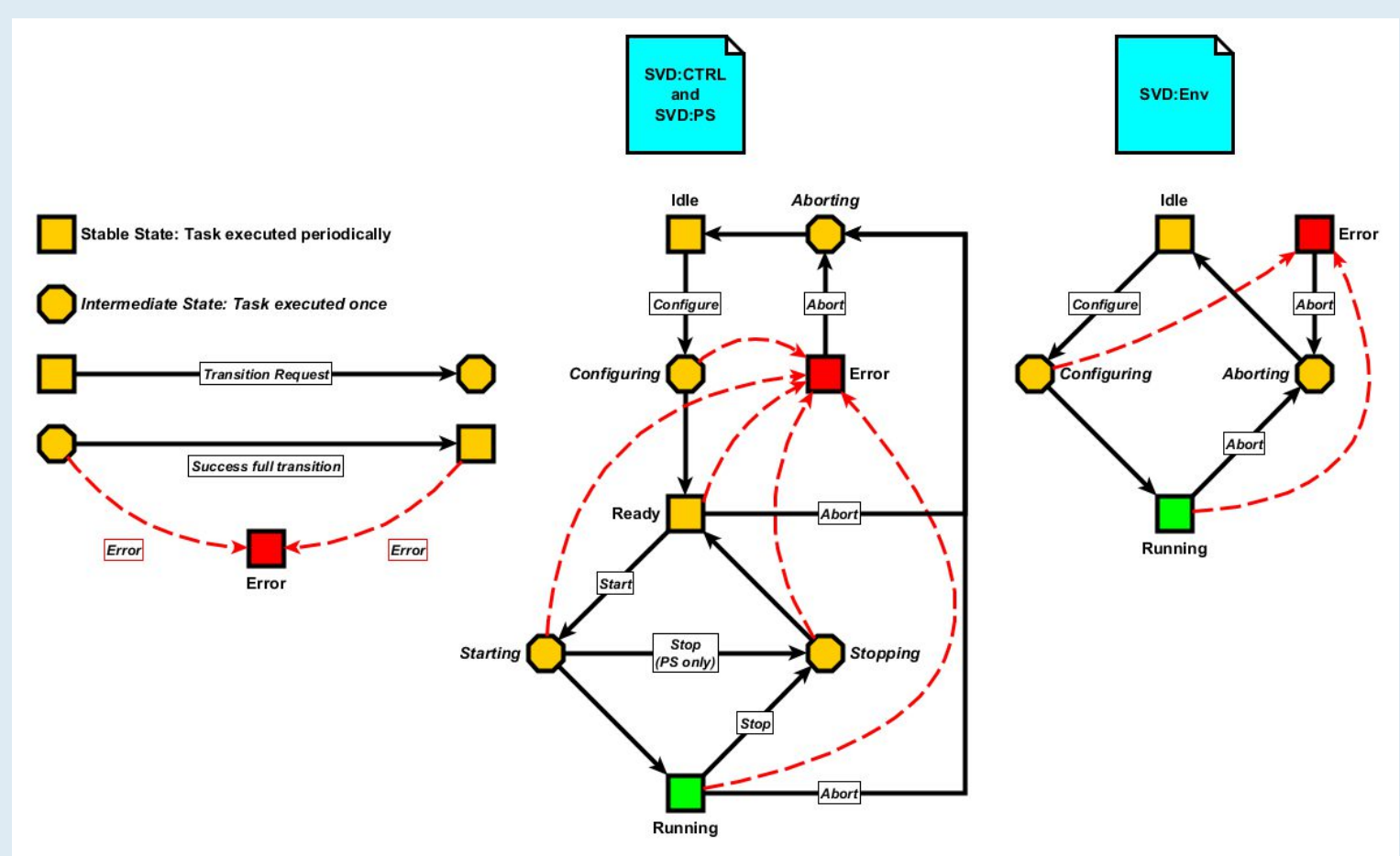
One half of SVD (+X half) attached to the beam pipe, which already carries the pixel detector in the center.

**Belle II Silicon Vertex Detector**  
Radii: 39 / 80 / 104 / 135 mm  
Sensors: 14 small rectangular DSSDs (124.88 x 40.43) mm<sup>2</sup>  
120 large rectangular DSSDs (124.88 x 59.60) mm<sup>2</sup>  
38 trapezoidal DSSDs at the slanted section 122.76 x (57.59-38.42) mm<sup>2</sup>  
Readout chip: APV25  
Shaping time: 50 ns  
Cooling: Two-phase CO<sub>2</sub> system (-20°C)



Overview of the SVD slow and run control system

**State Machines**  
As shown in the diagram, the SVD IOCs use two kind of state machines (SM). For environmental monitoring systems a rather simple SM with only two stable (Idle, Running) and two transitional states (Configuring, Aborting) is sufficient, while the more complex state machine is used for the SVD power supplies and the readout system.



State machines of RC IOCs (left) and ENV monitoring IOCs (right)

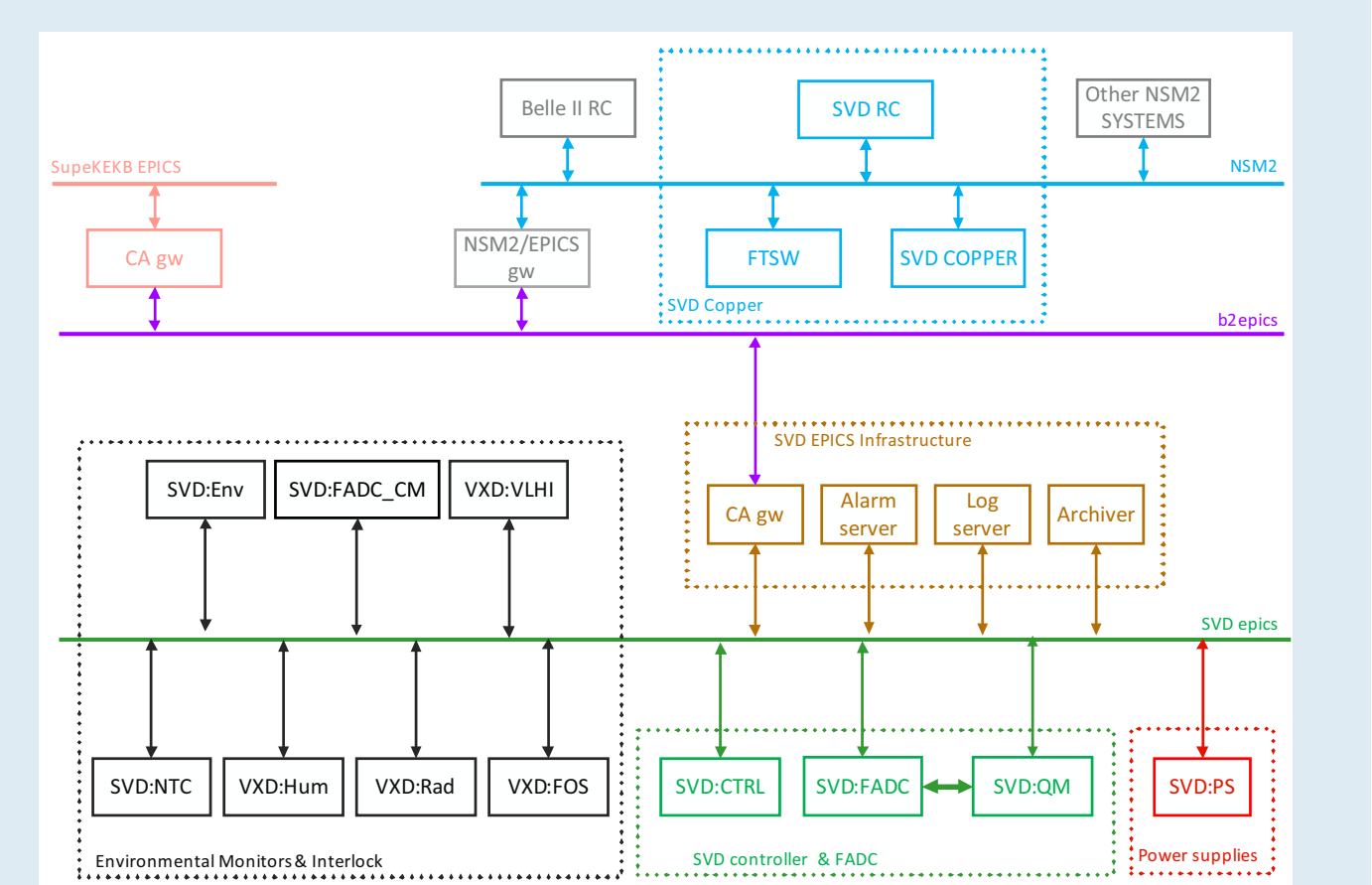
Transitions between the stable states are initiated by a request command from a parent IOC, e.g. the Belle II run controller. The parent's request is sent by a dedicated Request PV, while the state of the child is returned via a State PV. Thanks to these two dedicated PVs, it was possible to implement a quite simple handshake mechanism between parent and child IOCs. Once the state machine reached a stable state, it remains there and repeats its task until the next transition request is received. During the transition between two stable states, the state machine enters a transitional state, in which it performs a sequence of tasks, e.g. configuring the readout electronics or switching on power supply channels, but automatically proceeds to the next stable state after these tasks are finished. In case of an error condition, the state machine goes into error state, from which it has to be recovered by an abort request. In contrast to the ENV system, the IOCs of the power supplies (SVD:PS) and the readout electronics (SVD:FADC) use the more complex state machine with the three stable states Idle, Ready and Running. The transition between the states is again triggered and synchronised by request and state PVs.

Depending on the IOC, the three stable states of the RC state machine have the following meaning:

	SVD:PS	SVD:FADC	SVD:QM
Idle	LV off, HV off	off	off
Ready	LV on, HV off	configured	configured
Running	LV on, HV on (ramped up)	running and data taking	analysis ongoing

**SVD Slow and Run Control Overview**  
The SVD run and slow control system is implemented in EPICS (<https://epics.anl.gov>), a framework to build large-scale control systems. In EPICS, information exchange between sub-systems is realized via process variables, broadcasted on an Ethernet network. All hardware components are interfaced by dedicated input/output controllers (IOCs). In the SVD slow and run control system, all IOCs run on two servers, the RC/SC (run control / slow control) server and the ENV (environmental) Monitoring server, respectively. The RC/SC server hosts all IOCs, required to configure and operate the front-end and backend electronics, the CAEN power supplies as well as the SVD local run controller and the online data quality monitoring. On the ENV monitoring server, all IOCs to interface to the environmental monitoring systems, like temperature, humidity and radiation monitoring, the hard-wired interlock and the VME crate monitoring, are hosted. A further server is used to host EPICS services like the archiver appliance, a data logger and the alarm system. The operator PC is located in the control room and only hosts the graphical user interfaces. This server/client concept allows multiple connections to the system at the same time, e.g. local and remote operators can run their own instances of OPIs.

- SVD Copper:** Data transfer between readout electronics and central data acquisition.
- SVD controller & FADC:** Comprises main run controller (SVD:CTRL), IOC to configure and monitor SVD readout electronics (SVD:FADC) as well as spy data readout and online data quality monitoring (SVD:QM).
- Power supplies:** Configuration and monitoring of low and high voltage power supplies (SVD:PS).
- Environmental monitoring and interlock:** This group provides all the IOCs, which are required to acquire data from environmental monitoring sensors
  - SVD:Env Control IOC for all other ENV IOCs. inquires state from subordinated systems and propagates SW interlock to SVD:PS
  - SVD:NTC: Temperature of CO<sub>2</sub> cooling, measured by NTC sensors attached to cooling pipes and blocks
  - VXD:FOS: Temperature of SVD ladders, measured by fiber optic sensors, located below readout chips
  - VXD:Hum: Humidity of VXD dry volumes
  - VXD:Rad: Radiation dose from diamonds radiation sensors
  - VXD:VLIH: Interface to the VXD hardwired interlock system
- EPICS infrastructure:** archiver appliance, alarm system, message logger, gateway, etc.



Block diagram of the SVD IOCs

**1 SVD PS - CAEN Crate #1**: Merged Channel Status, Crate Infos, System States.

**2 SVD Overview**: System States, Forward/Backward status, SVD Local Status, Global Status.

**3 SVD VME Crate 0**: System States, Measured fan speeds, Air temp, Conf. Speed, PS status.

**4 SVD Local Control**: SVD:CTRL, SVD:PS, SVD:FADC, SVD:QM, SVD:Env, SVD:NTC, VXD:FOS, VXD:Rad, VXD:VLIH.

**5 SVD Ladder 5.4**: System States, BW Data Errors, Z Data Errors, CE Data Errors, FW Data Errors, BW FADC Monitor, Z FADC Monitor, CE FADC Monitor, FW FADC Monitor.

**6 Selection of SVD RC/SC OPIs:**

- 1) Power Supply status
- 2) General SVD status
- 3) VME crate status
- 4) Local SVD controller
- 5) Ladder details
- 6) Calibration peak plots
- 7) Ladder summary of FOS temperatures
- 8) FOS temperatures history
- 9) VXD hardwired interlock
- 10) Cooling tube temperatures
- 11) FOS temperature of all layer 6 ladders

**7 VXD FOS Temperatures**: Layer 6, Layer 5, Layer 4, Out Cover, PXD (L), BW DSSD, Ambient.

**8 Temperature history plot of layer 4 fiber optic sensors**: History Plots.

**9 VXD Hardwired Local Interlock**: INPUT SIGNALS, NTC Interlock, Dew Point, Water Leak, Dock Chiller, Flow rate (GPM).

**10 NTC Temperatures**: X BWD, X FWD, X Origin, IBelle, CO2 Tubes, Dock Chiller.

**11 Temperatures of all L6 fiber optic sensors**: Detailed sensor data table.

All graphical operator interfaces (OPI) of the SVD run and slow control are designed with Control System Studio (CSS, [http://controlsystemstudio.org/page\\_about.html](http://controlsystemstudio.org/page_about.html)), an Eclipse-based tool to create large-scale control systems. It directly interacts with the underlying EPICS network to get and/or set the PV values. The integrated data browser can retrieve the history of each PV from an archiver appliance and thus allows easy generation of history plots for all archived PVs. The Belle II SVD OPIs are divided into two categories, the first for RC, power supplies and data quality monitoring and the second group for environmental monitoring sub-systems. The SVD Overview OPI is the entry point of the run and slow control, which provides an overview about the general state of the SVD. It displays the overall status of all sub-systems, each SVD ladder, power supplies, VME crates as well as general information from Belle II run control, like experiment and run numbers, trigger and data type, etc. From here the operator can navigate to other OPIs with more detailed information about each SVD ladder, power supplies and the back-end electronics. It is also possible to access detailed plots with condition data, like pedestal, noise, hitmap, SNR for each individual sensor (see pic. 6). SVD Local Control OPI (see pic. 4) is foreseen to operate in local run mode, when the SVD is excluded from the Belle II run control. This local operation mode is used to retrieve and calculate all calibration constants, which are required for data taking and offline data analyses. Apart from the RC/SC OPIs, there is a dedicated OPI for each environmental monitoring sub-system, as shown in pic. 7, 9 and 10. These OPIs also allow navigating to further views with more detailed information and history plots of the systems, e.g. the temperatures of each fiber optic sensor (see pic. 8 and 11).

\* Email: christian.irmeler@oeaw.ac.at