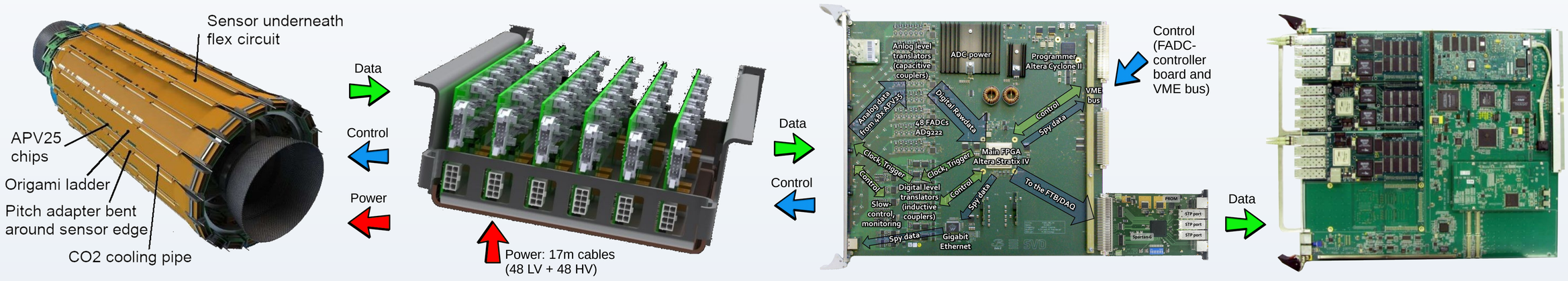
15th Vienna Conference on Instrumentation, from February 18-22, 2019
Richard Thalmeier (HEPHY Vienna) for the Belle II SVD Group

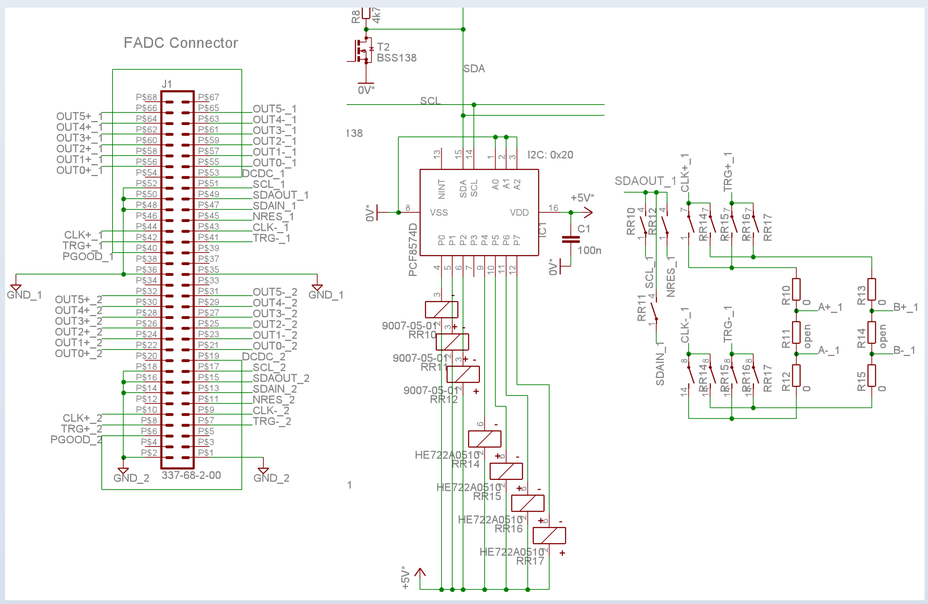
Series Production Testing, Commissioning and Initial Operation of the Belle II Silicon Vertex Detector Readout System



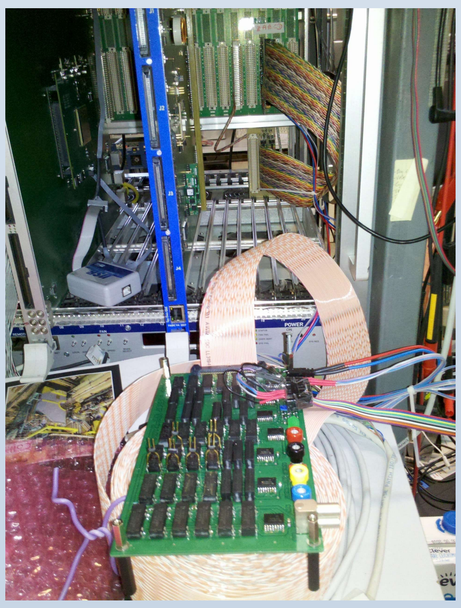
Silicon Vertex Detector (SVD): Front-end hybrids with 1748 APV25 chips, 128 channels each, on 172 sensors in 4 layers; output: time multiplexed analog voltages	344 2.5m copper cables, á 50 wires	8 junction boxes, 6 junction boards (JBs) each, with rad-hard and magnetic tolerant DC/DC converters, inside the detector housing	192 13m copper data cables, á 68 wires	52 Flash Analog Digital Converter (FADC) boards in 4 crates, on top of the detector structure	52 Finesse Transmitter Boards (FTB), plugged into P3 of the FADCs	52 optical data links (>20m)	DAQ system, which further sends the data to servers

The Silicon Vertex Detector (SVD) of the Belle II experiment at the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan, consists of 172 double-sided micro strip technology silicon sensors arranged cylindrically in four layers around the interaction point. A total of 1748 readout chips (APV25) process and send the analog signals over 2.5 meter long copper cables to 48 Junction Boards (JBs) located inside the detector housing which provide an interface for connecting the cables on the inside of the detector with those of the outer world, and to power the detector with radiation-hard and magnetic insensitive DC-DC converters. From there the analog data are sent over 13 meter long copper cables to 52 A/D Converter boards (FADCs) located in crates on top of the Belle II detector structure. They control the detector, convert the SVD data into digital domain, and perform first data processing using powerful FPGAs. From the FADC boards the data are then sent out to optical converter boards (FTBs) and to the central DAQ by optical fibers.

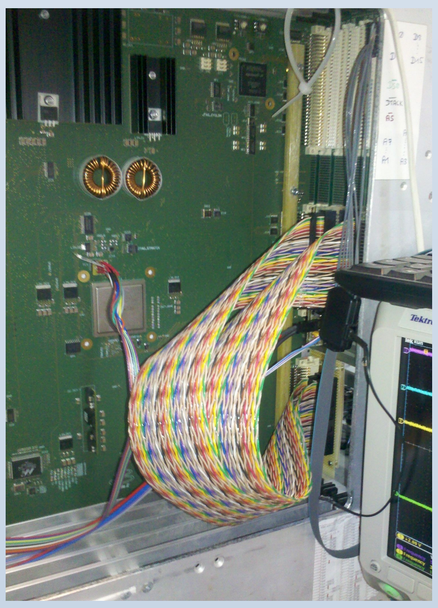
The Junction boards and the FADC boards were developed by HEPHY Vienna, and assembled by a company, also in Vienna. They were optically tested at this company, but not electrically, which is why a test system had to be implemented which tests all the components, interconnections and connections on these boards. Including spares there are more than 60 boards each. So this testing had to be designed to be performed at least partially automated, so that for example some testing hardware equipment is to be connected to the device under test, a test firmware is flashed onto the board, a button is clicked on a PC and the test result is being presented. No oscilloscope or multimeter is needed. The testing procedure is designed to not require much acknowledgment of the detailed internals of the hard- and firmware, so it can be performed also by people who were not involved in the hardware development, by following a well-defined step-by-step instruction manual.



Small fractions of the schematics of the FADC board tester PCB used to automatically examine the FADC series production. The input signals are generated digitally by the main FPGA (with respective firmware) on the FADC board and switched to the analog-digital converter ICs using reed relays controlled by the FPGA via an I^2C bus



FADC board tester (analog part)



FADC board tester (digital part)

FADC board tester: two histograms and a mean value graph of ADC data on square wave inputs

Junction board tester

The first tests on all boards are thermal inspection using an infrared camera and power consumption, measured using the internal current monitors of the VME crates for the FADC boards and laboratory power supplies for the junction boards.

For the FADC boards a special test hardware together with firmware for the on-board FPGA and software for the PC controlling the VME bus has been developed. The “P1” connector and the inner rows of the “P2” connector to the VME bus are tested using VME transfers. The remaining digital pins of the “P2” connector as well as those of the “P3” connector are inter-connected with a special cable, which connects each LVDS input to an LVDS output. Since the amount of outputs does not exactly match the one of the inputs, some test pins on the FADC board are used additionally. The firmware sends 1024 pulses to one single output at different frequencies up to 40 MHz. Independent counters enumerate the signal changes on all inputs individually at the same time. The results are then read out and interpreted by the software. If the input connected to the active output counted any other number than 1024, or if any other input counted anything else but zero, the test has failed, and the faulty line gets reported. The same is then done for all other lines on these two connectors successively, and also for some digital signals of the front connectors like the power-good and enable signals of the DC/DC converters on the junction boards. All this digital testing only needs a few seconds per board.

The analog inputs for the detector signals are tested in a different way: The differential input line pair of each flash analog digital converter can be switched to one output of two voltage dividers, or to both of them at the same time, using reed relays controlled by I^2C chips which are controlled by the FPGA, the firmware and the software. These two voltage dividers are powered by a digital LVDS output line pair of the FADC boards each. So the FADC input lines can be fed by rectangular signals with three different voltage levels of 0 and 1, as well as different frequencies and duty cycles. The DAQ then records histograms of the ADC outputs. The shapes of these histograms are automatically analyzed by the software which allows precise judgment about the performance of the individual analog-digital converter. By changing the delay values of the “delay25” ICs on the FADC board in the clock lines of the ADCs also these chips are tested along the way.

The remaining lines on the front connectors are slow control signal inputs like voltage and temperature monitors. They are simply tested by feeding them with different voltages generated by different voltage dividers also switched by reed relays. They are converted to 24 bit digital data by sigma-delta ADCs which the software reads and compares to the nominal levels. The JTAG connectors are tested using an USB blaster to flash and verify the EEPROMs of the two FPGAs (which additionally is verified by rebooting in the procedure), the onboard JTAG flasher by flashing the Stratix FPGA via the Cyclone FPGA, and the Gigabit Ethernet by sending and receiving packets to and from a PC.

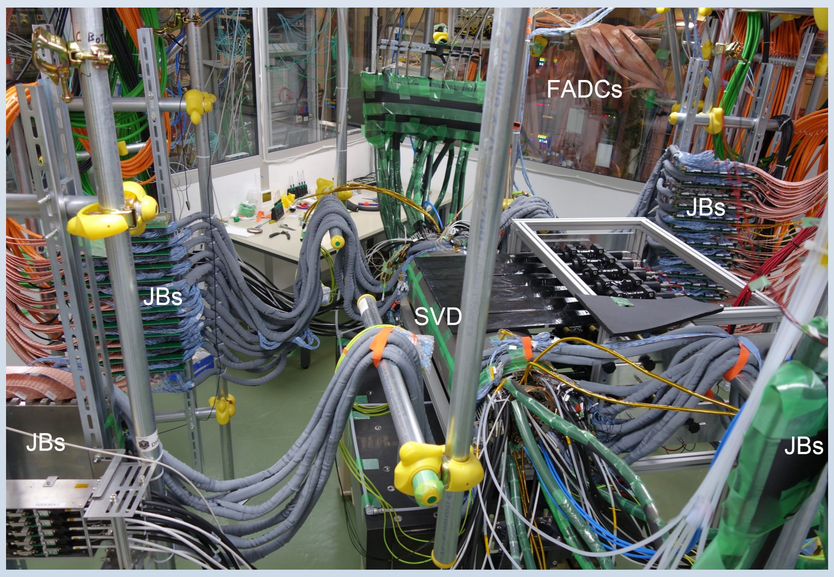
On these tests some component populating errors have been detected, like a few so-called tombstone SMD resistors and capacitors (where only one side of the component is soldered properly), one clock distributor IC soldered twisted by 180 degrees, one FPGA with badly soldered BGA connectors, and the like. These failures have been successfully repaired, and all boards behaved well afterwards.

The junction boards and all cables are tested using a commercial cable tester which measures resistances and capacities as well as diode characteristics between any combination of its connectors and so compares the whole board to a stored sample. For the DC/DC converters we developed and built a board which measures and displays the voltages. Only a few minor errors have been found, and they have been corrected on-the-fly.

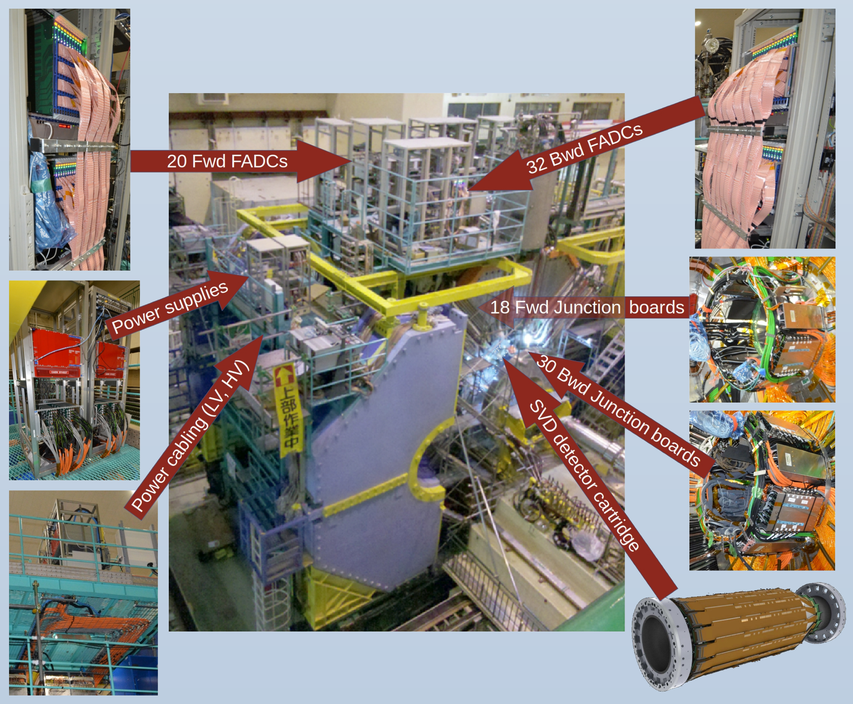
In a second pass each FADC gets connected to a junction board and to a class B L5 detector ladder one after the other. The separation of the sensor bias voltage (“HV”) on the FADC boards, the cables and the junction boards are tested using a ±200V power supply with current measurement, and all channels of the ladder are read out by the DAQ PC. This procedure (but without the HV power supply) is repeated later for each channel every time before the final detector gets connected to the system.

After all the boards were tested individually twice (once in Vienna, and once at KEK in Japan) using this test procedure, the whole readout system with all the final boards and the final detector has been tested in two commissioning setups in the basement of the detector hall in 2018, and afterwards, in December 2018, in the final detector structure.

In January 2019, Phase 3 operation has started and the SVD system is running stable and reliably.



Last commissioning setup before mounting into the Belle II detector structure using the real SVD and only final electronic components. (FADC crates are located outside the clean-room



Final installation and in-system tests of all the components

Belle II
SVD

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