Development of a FE-I4-based module for radiation monitoring with BEAST II during the commissioning phase of the Belle II detector

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I hereby declare that this thesis was formulated by myself and that no sources or tools other than those cited were used.

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Contents

Introduction

Questions about the origin and characteristics of the universe are part of human nature. The Standard Model (SM) of particle physics describes the fundamental particles, divided into quarks and leptons, and the force carriers of the strong, weak and electromagnetic interaction, called gauge bosons. It is known that the SM, in particular at high energies, cannot be complete. Several theories beyond SM [1] have been proposed but can only be verified by experimental evidence.

In order to stress test the SM, multi-layer-detectors are used in collider experiments to analyse the physical process behind the collisions and extensive simulations of the underlying physical theory are performed.

KEK (engl.: High Energy Accelerator Research Organization) in Tsukuba, Japan, performs research in high-energy physics with its main installation, the electron-positron accelerator SuperKEKB. A better understanding of flavour-changing processes in the weak interaction is supported by studies focussing on particle decays including b-Quarks. Especially measurements on CP[1]-violating processes in the Standard Model and on the CKM[2]-Matrix elements are possible. Among other research topics, detailed studies in the B-Meson analysis were conducted at the Belle-experiment [2]. The Belle detector has recorded a dataset of e^+e^-- collisions on the $\Upsilon(4S)$-resonance from 1999 to 2010 with an integrated luminosity of $1\,\mathrm{fb}^{-1}$ at the KEKB accelerator. The resonance is an excited state of $b\bar{b}$ which almost decay exclusively into two B-mesons, and this is of particular interest for CKM-element measurements.

Since 2010, the accelerator has been upgraded with the goal of an instantaneous luminosity 40 times higher compared to KEKB. At an asymmetric energy of colliding electrons and positrons, the new Belle II detector will record the resulting events. Before the installation of the Belle II inner detector in 2017, the BEAST II (**B**eam **E**xorcisms for **A St**able Experiment) experiment has been developed for the study of background radiation during the commissioning phase of the SuperKEKB machine. The experiment will measure the expected radiation for the components of the inner detectors and support the tuning of the accelerator beam optics and collimator system.

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[1] Charge-Parity
[2] Cabibbo-Kobayashi-Maskawa

In the inner detector volume, the BEAST II experiment will consist of five complementary detector systems: FANGS (**FE-I4 A**TLAS **N**ear **G**amma **S**ensors), CLAWS (s**C**intillation **L**ight **A**nd **W**aveform **S**ensors), PLUME (**P**ixelated **L**adder using **U**ltra-light **M**aterial **E**mbedding) and a segment of the vertex detector.
Within the scope of this thesis, the development and composition of the FANGS detector as well as its operation are being discussed.
The following sections of this chapter deal with the theoretical and technical background information needed for the basic understanding of the operation of this detector.

In Chapter 2, the BEAST II experiment is described and each detector system is explained. The section about background radiation covers the origin and impact of the expected backgrounds.

Chapter 3 provides an in-depth overview on all components of the FANGS detector. It starts with the manufacturing steps of the modules, followed by the description and characteristics of the components. As the data acquisition is mandatory for the detector, it is explained in detail. The chapter closes with the test set-up used for the measurements in this thesis.

The measurements using the FE-I4 are presented in Chapter 4. It describes the characterization of the FANGS stave, including the required tuning steps of the Front-End electronics, and it concludes with the calibration carried out with radioactive sources.

Investigations about the behaviour of the FANGS modules under realistic conditions are carried out in two separate chapters. Chapter 5 presents the irradiation campaign of the LVDS driver, an industrial component implemented on stave for data transmission. The cooling concept of the final experiment is discussed in Chapter 6, including thermal tests.

Chapter 7 is dedicated to the integration of the detector systems in the inner detector volume, highlighting the mounting sequences of BEAST II.

The final Chapter 8 summarises the results presented in this thesis and gives an outlook on further developments.

1.1 The SuperKEKB accelerator

The asymmetric electron-positron accelerator SuperKEKB [3] is the upgrade of the KEKB machine in Tsukuba, Japan. The new accelerator operates in the same tunnel system as KEKB, using a Low Energy Ring (LER) for positrons and a High Energy Ring (HER) for electrons. An overview of the accelerator is shown in Fig. 1.1.
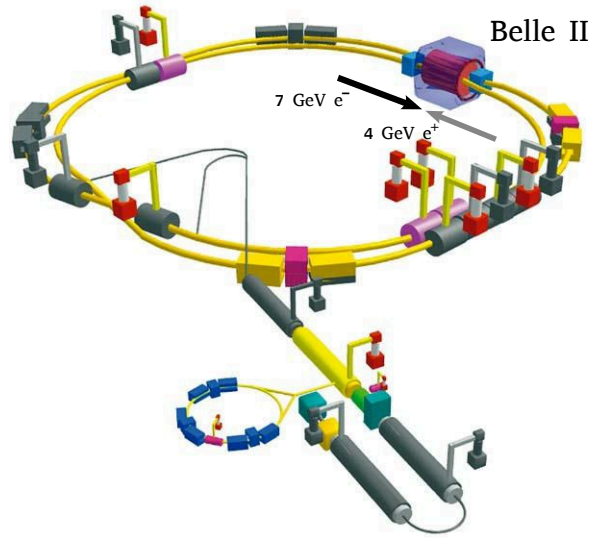

Figure 1.1: Overview of the SuperKEKB accelerator and the location of the Belle II detector. The Belle II detector encloses the interaction region where electrons and positrons collide [4].

The major amendment of the upgrade involves the increase of luminosity. The instantaneous luminosity $\mathcal{L}$ with two bunches containing n_1 and n_2 particles can be written as [5]:

$$\mathcal{L} = f \cdot \frac{n_1 n_2}{4\pi\sigma_x\sigma_y}.$$ (1.1)

The collision frequency and the transverse beam sizes in the horizontal and vertical direction are characterized by f and $\sigma_{x,y}$, respectively. In the upgrade, the beam currents are increased, i.e. for the LER from 1.6 A to 3.6 A and for the HER from 1.2 A to 2.6 A. Additionally, the size of the beam is squeezed to a vertical beam size of 0.048/0.062 μm (LER/HER), called the nano-beam scheme [6]. These changes will provide an instantaneous luminosity of $8.1 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ which is a factor of 40 higher than the peak luminosity at KEKB. The energy of the positrons $E_{e^+} = 4\,\mathrm{GeV}$ and the electrons $E_{e^-} = 7\,\mathrm{GeV}$ result a center of mass energy of [7]:

$$\sqrt{s} = 2 \cdot \sqrt{E_{e^+}E_{e^-}} \approx 10.58\,\mathrm{GeV}.$$

The resultant center of mass energy is chosen to hit the production of the Υ(4S) resonance. With the old energies of HER/LER of 8 GeV/3.5 GeV the boost acting on the produced particles was $\beta\gamma = 0.42$. Compared to KEKB, the energy difference between the LER and the HER will be reduced, effecting the reduction of the boost acting on the Υ(4S) resonance. The increased energy of LER and decreased energy of HER reduce the boost to:

$$\beta\gamma = 0.28.$$

In order to compensate for closer decay vertices, the resolution of the detector needs to be increased. The decreased boost and the high particle rate require a complete renovation of the detector and its data acquisition system. In the next section, the Belle II detector is described.

1.2 The Belle II detector

The Belle II detector is designed for high precision measurements at the SuperKEKB accelerator. With the upgrade of the KEKB to the SuperKEKB, it is necessary to adjust the detector to higher event and background rates. A schematic representation of the Belle II detector is shown in Fig. 1.2. The region where the electrons and positrons collide is called interaction region (IR) and is surrounded by the detector.
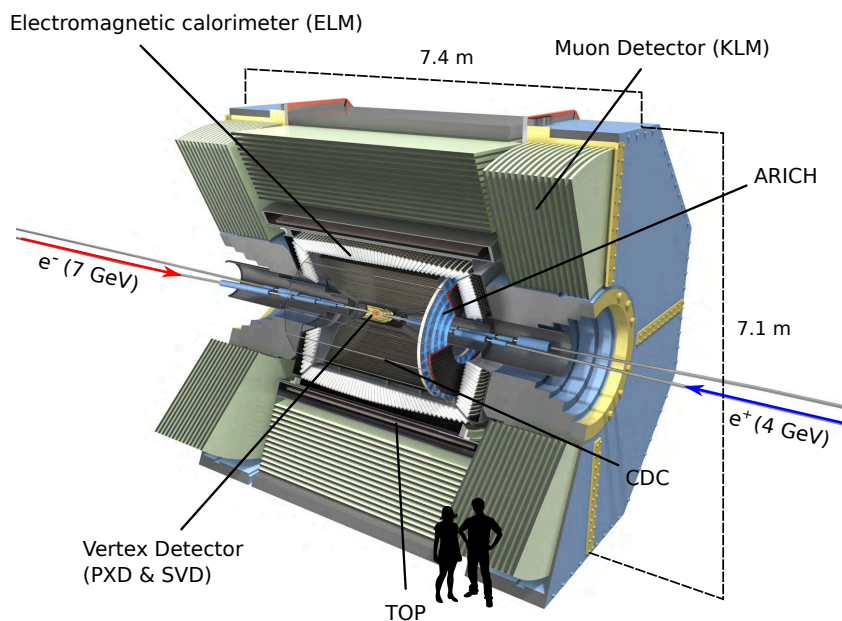

Figure 1.2: The schematic representation of the Belle II detector showing the various sub-detectors. The detector surrounds the interaction region where electrons and positrons collide [8].

The detector is separated into three regions which belong to different angles with the beam axis: The forward, barrel and backward region are hermetically covering the IR to detect the boosted decay products of the typical $\Upsilon(4S) \rightarrow B\bar{B}$ reaction. In the inner volume of the detector,

a superconducting solenoid magnet provides a constant magnetic field of 1.5 T to bend the tracks of charged particles for momentum determination.

The sub-detectors of Belle II are customized for tracking, identifying and measuring the momentum and energy of the different particle types in order to reach a precise reconstruction of the event. A short summary of the main sub-detectors is listed below. The list is in order of increasing distance from the interaction region.

- **Pixel Detector (PXD)**
  The first detector surrounding the interaction region is the PXD. The detector concept is based on the DEPFET[1] [9] technology. Each pixel contains a Field Effect Transistor, integrated in a fully depleted silicon bulk. With its very thin sensors (75 μm) it has a low material budget (0.2 % X_0 per layer). 8 million pixels are distributed over two layers providing position sensitive measurements with an impact parameter resolution of 15 μm. The two layers have a distance of 14 mm and 22 mm from the IR.

- **Silicon Vertex Detector (SVD)**
  The SVD [10] consists of four layers of Double-Sided Silicon Strip Detectors (DSSDs) and provides a precise vertex determination in connection with the PXD. A fast readout is supported by the Front-End chip with a waveform shaping time of 50 ns. The average material budget is 0.6 % X_0 per layer.

- **Central Drift Chamber (CDC)**
  The CDC [11] is a gas filled volume with charge collection via 14 336 electric wires with a thickness of 30 μm. It allows charged track reconstruction and momentum measurements with a track efficiency above 90 % from 0.5 to 2.5 GeV. In addition, particle identification is possible due to the energy loss of particles flying through the sub-detector.

- **Particle identification system (PID)**
  The PID [12] consists of the Time-Of-Propagation detector (TOP) and the Aerogel Ring Cherenkov detector (ARICH) located in the barrel region and in the forward endcap, respectively. Both systems are based on the Cherenkov effect for particle identification and provide the discrimination between $K^\pm$ and $\pi^\pm$ in a wide momentum range.

- **Electromagnetic calorimeter (ECL)**
  The ECL [13] surrounds the PID and consists of CsI(Tl)-scintillators coupled to photo-detectors. The system is subdivided into the forward, barrel and backward region. The energy measurement of electrons, positrons and photons is provided in this sub-detector. The energy and angle of photons can be determined from 20 MeV to 4 GeV.

- **K_L and muon detector (KLM)**
  The outermost sub-detector of the Belle II detector is the KLM [12]. It distinguishes between K_L and muons using Resistive Plate Counters (RPCs). In addition, momentum measurements of muons are supported.

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[1] DEpleted P-Channel Field Effect Transistor

1.3 Hybrid pixel detectors

A Hybrid pixel detector is constructed as a two-unit structure with a pixelated sensor for particle detection in a first layer and a readout chip for the processing of the signal in a second layer. Solder bumps [14] and flip-chip techniques [15] are building the connection between the signal generating part and their processing.

Hybrid pixel detectors are characterized by their precise time and spacial resolution with the feature of high radiation resistivity so that they are implemented in experiments close to the interaction region where the highest amount of radiation is generated.

In Sec. 1.3.1, the working principle of the silicon sensor is explained, followed by an overview of the readout electronics in Sec. 1.3.2.

1.3.1 Planar silicon sensor

The silicon sensor is a basic element of a hybrid detector and different design concepts are available for the sensor structure.

In the scope of this thesis, **planar n-in-n silicon sensors** are of particular interest. This type of sensor uses n-doped regions in which impurities are introduced to change the properties of the intrinsic silicon. Silicon is doped with elements as electron donors or acceptors e.g. boron (B) and phosphorus (P), respectively [16]. Doping with electron donors is called n-doping, providing an increase of negative charge carriers. Doping with electron acceptors leads to an increased number of positive charge carriers, referred to as p-doping.

The planar pixel sensor is divided into three parts. The frontside consists of highly n^+ doped **pixel implants** structure. The backside is an unstructured, highly doped p^+ implant. The silicon bulk between the two regions has a high resistivity which is lowly n doped. A depiction of the described structure is illustrated in Fig. 1.3.
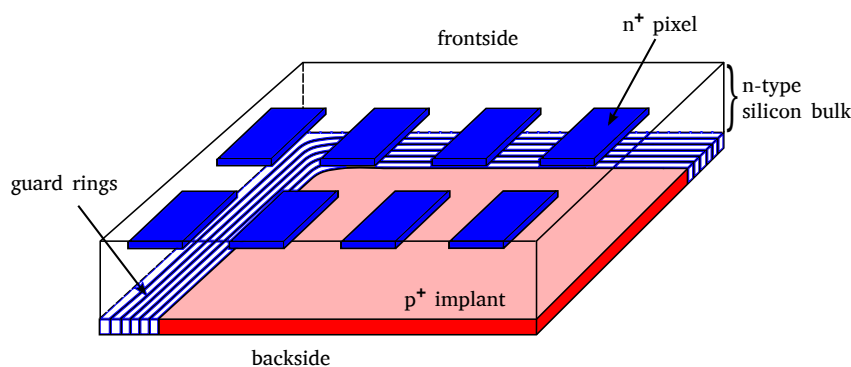

Figure 1.3: Illustration of an n-in-n planar silicon sensor.

In addition, to have control over the voltage at the edges, **guard rings** are implemented on the backside. The guard ring structure is placed between the p^+ implant and the edges of the sensor to induce a smooth voltage decrease from the active area to the edges.

Biasing and charge collection

In case of an n-in-n sensor, an external negative bias voltage is applied to the p$^+$ implantation, while each pixel on the frontside is grounded. This voltage extends a volume free from charge carriers in the silicon bulk, called the **depletion zone**. The process is depicted in Fig. 1.4.
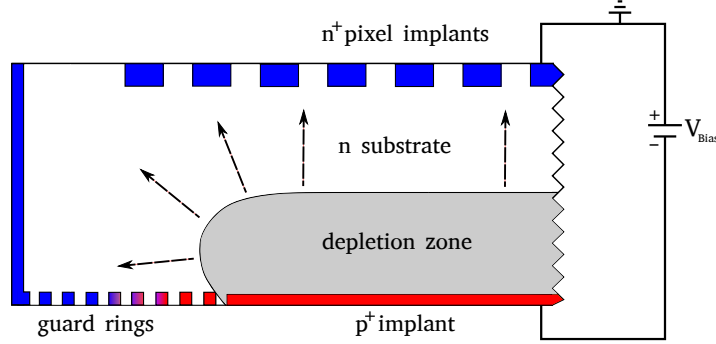

Figure 1.4: Simplified cross section of an n-in-n sensor. The applied bias causes an increase of the depletion zone and is extended to the entire volume.

The applied voltage V_{Bias}, also called High Voltage (HV), induces an electric field from the p$^+$ implantation to the n$^+$ pixel implants. In order to calculate the spread of the depletion region into the bulk material, the depletion depth d is described by [17]:

$$d = \sqrt{\frac{2\epsilon_0\epsilon_S(N_A + N_D)}{qN_AN_D} \cdot (V_{\text{Bias}} + V_{\text{bi}})}\,, \tag{1.2}$$

with ϵ_0, ϵ_S as the permittivity in free space and in the semiconductor, respectively. N_A and N_D describe the doping concentrations of the acceptor and donor material.

Since the built-in voltage V_{bi} is negligible ($\sim$0.7 V) to V_{Bias} and in the case of an asymmetric doping ($N_A \gg N_D$), the depletion depth d can be thus approximated:

$$d \approx \sqrt{\frac{2\epsilon_0\epsilon_S}{qN_D} \cdot V_{\text{Bias}}}\,. \tag{1.3}$$

If the bias voltage is high enough, the entire silicon n-substrate is completely depleted from free charges.

At an average energy of 3.65 eV [18], ionizing particles, e.g. photons, are able to generate electron-hole pairs. The electrons, which are the majority carriers in this type of sensor, drift towards the electrodes as shown in Fig. 1.5.
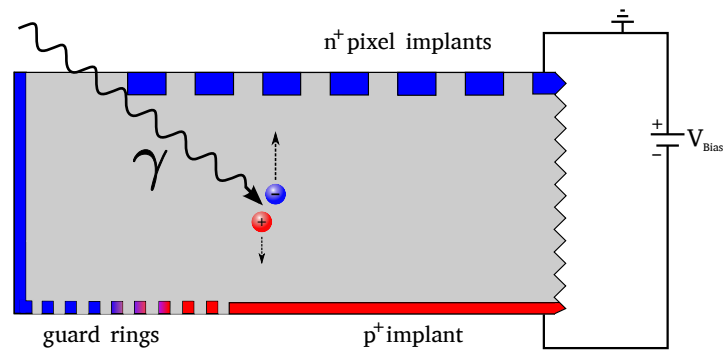
Figure 1.5: An incoming photon generates an electron-hole pair in the silicon sensor. The electron and hole drift to the n^+ pixels and p^+ implant, respectively.

The number of primary originated charge carriers are proportional to the deposited energy of the particle. The generated signal from the sensor has to be extracted, amplified and digitized. This is accomplished by a connection of each pixel to its own readout circuitry on the Front-End electronics via a solder ball.

1.3.2 FE-I4B Front-End readout chip

The FE-I4B is a Front-End (FE) readout chip with a size of $18.8 \times 20.2\,\text{mm}^2$. The Front-End readout system allows the simultaneous signal processing of 26 880 pixels. The Front-End is divided into 80 columns with 250 µm pitch and 336 rows with 50 µm pitch and is designed in an IBM 130 nm feature size bulk CMOS[1] process. This readout chip is also used in the ATLAS Insertable B-Layer (IBL) pixel detector modules [19] with its feature of fast data processing and radiation hardness. A picture is shown in Fig. 1.6.
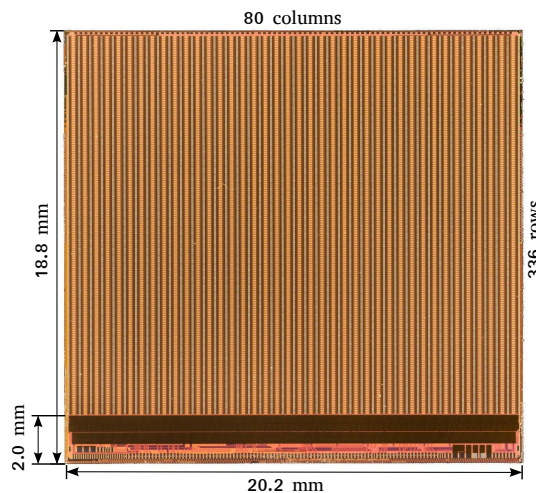
Figure 1.6: Picture of the FE-I4 readout chip with 80 columns and 336 rows. With a pixel size of $50 \times 250\,\text{µm}^2$ for 26 880 pixel, it has an area of $380\,\text{mm}^2$ [19].

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[1] Complementary Metal–Oxide–Semiconductor

Each cell of the FE-I4 readout chip is connected to a sensor pixel, using bump bonds. Therefore, each pixel has its own analog pixel cell, depicted in Fig. 1.7.
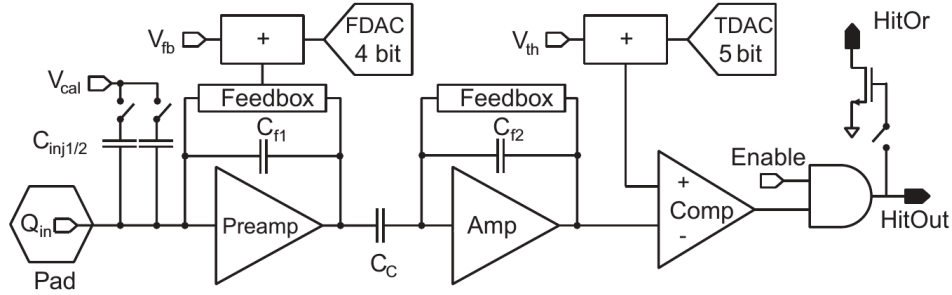

Figure 1.7: Schematic of the analog pixel cell in the FE-I4. Each sensor pixel is connected to its own analog pixel cell [20].

The signal of resulting electrons in the sensor is collected at a pad (Q_{in}). A two-stage charge-sensitive amplifier (CSA) in an AC-coupling provides the shaping and voltage gain of the signal in front of a discriminator. The shaping time of the preamplifier (Preamp) and the threshold of the discriminator can be adjusted with V_{fb} and V_{th}, respectively. The configuration of these global settings affects all pixels in the matrix.

An individual feedback for the discharging current (4-bit FDAC) and the threshold of the comparator (5-bit TDAC) is present in each pixel and allows independent fine tuning. The amplitude of the amplifier output is proportional to the deposited energy in the sensor. After the CSA, the signal is compared to the threshold of the discriminator and sampled with the supplied 40 MHz clock yielding the **ToT** (Time-over-Threshold). The digital output implies a hit of the detector, and the digitization is stored until it is read out by the data acquisition system.

Moreover, it is possible to connect the output (HitOut) to the HitOr bus which is routed to each pixel of the FE matrix using a logical OR. The bus can be used to sample the ToT of the pixel carrying the highest collected charge, thus the longest ToT, with a faster clock of 640 MHz provided by an Field-Programmable Gate Array (FPGA). This technique is called **TDC**-method (Time-Digital-Converter). The increased resolution from 4-bit (ToT) to 12-bit (TDC) improves the resolution of the charge signal [20],[21]. In addition, the hit bus can be used as an internal trigger (see Sec. 3.5.2).

For tuning and calibration purposes, a charge injection circuit is located in every pixel cell of the readout chip using the calibration voltage (V_{cal}) and two injection capacitances $C_{inj1/2}$. The injected charge is given in units of voltage steps per DAC[1] (PlsrDAC). Further relevant specifications of the FE-I4 are listed in Tab. 1.1.

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[1] Digital-to-Analog Converter

Item	Value
Pixel size	$50 \times 250 \, \mu m^2$
Maximum injected charge	$100000 \, e^-$
Radiation Tolerance	$300 \, Mrad$
Operating temperature range	$-40\,^{\circ}C$ to $+60\,^{\circ}C$
Average hit rate with $< 1\,\%$ data loss	$400 \, MHz/cm^2$
Maximum sustained trigger rate	$200 \, kHz$

Table 1.1: FE-I4 specifications [22].

The BEAST II experiment

The upgrade from KEKB to SuperKEKB includes the increased luminosity and the reduction of beam spot sizes. Therefore, the Belle II detector has to face not only higher rates of events but also an increased background radiation depending on luminosity, beam size and beam currents compared to the previous experiment. In the commissioning phase of the previous Belle detector, the first version of the SVD had upcoming problems with soft X-rays from synchrotron radiation [23]. Besides that, the neutron background was unexpectedly problematic in Belle. Several effects can degrade or stop the performance of the sub-detectors: Surface damage and bulk damage due to ionizing and non-ionizing radiation, respectively and data loss because of high occupancies resulting in a reduction of the vertex reconstruction efficiency [24].

The necessity of having tolerable background levels before the installation of the Belle II inner detector pushed the idea of the BEAST II experiment, a detector system for the commissioning of the SuperKEKB accelerator. The main purpose of BEAST II is to measure the **instantaneous** as well as the **integrated radiation dose**, the Belle II vertex detector will be exposed to. Another important aspect is that the BEAST II detector will help to optimally **tune the accelerator**, including beam optics and the collimator system. The SuperKEKB machine requires measurements of the luminosity and background levels in real time to tune the beam optics. The BEAST II detector will collect data in the Belle II environment, paving the way to avoid damage of the new vertex detector. Outside the volume, micro TPC[1] detectors, He-3 tube detectors and PIN-diodes will provide additional measurements in the experiment. In this thesis, the focus is on the sub-detectors located in the VXD volume. The layout of the experiment is depicted in Fig. 2.1.

The BEAST II experiment follows the same coordinate system as the Belle II detector. The x-axis and the z-axis define the horizontal plane of the experiment in which the positive x-axis points in the direction outside of the accelerator ring. The z-axis is pointing along the electron beam. Finally, the y-axis is vertical upward. In addition, there are the azimuthal angle ϕ and the zenith angle θ to describe the full space. ϕ describes rotations in the xy-plane and θ angular dependencies in the yz-plane. The five sub-detectors of BEAST II are described below.

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[1] Time Projection Chamber

- **PXD and SVD:** In the positive x-direction at $\phi = 0°$, there are two PXD and four SVD layers using the same modules and data acquisition system as in the final Belle II experiment. The rest of the VXD volume is covered with three radiation monitor systems.
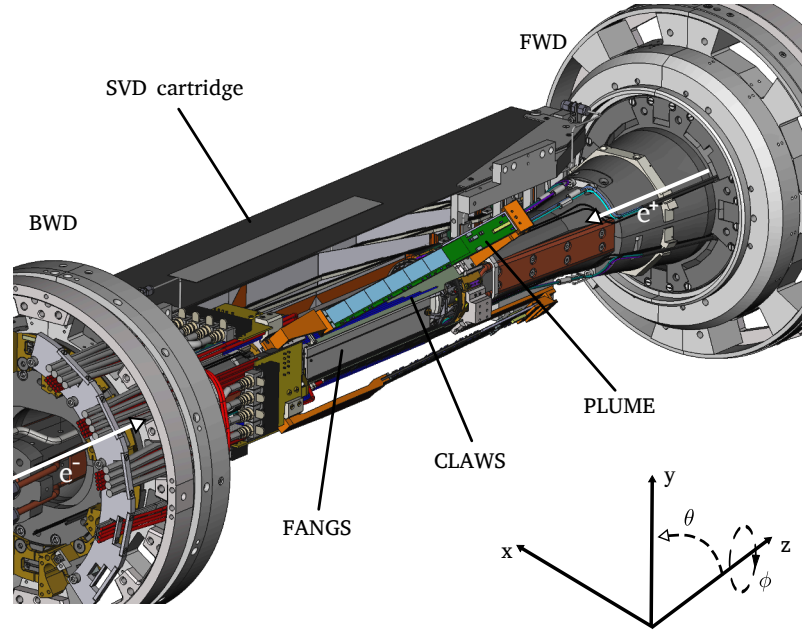

Figure 2.1: Layout of the BEAST II experiment in the volume of the VXD. Two layers of the PXD are followed by the SVD cartridge, containing four layers of DSSD. FANGS, CLAWS and PLUME fill the remaining space around the beam pipe at the interaction region. The forward (FWD) and backward (BWD) regions of the detector are also shown [25].

- **FANGS:** Three FANGS staves are set at the distance of 22 mm from the IR at $\phi = 90°, 180°$ and $270°$, covering the entire acceptance in θ between $17°$ and $155°$. For the background measurements, the sensors of FANGS are sensitive to low keV X-rays and high particle rates using hybrid pixel sensors from the ATLAS IBL modules. In the course of this work, the FANGS detector is developed and in detail discussed in Chap. 3.

- **CLAWS:** The gap between the FANGS staves is filled by two CLAWS detectors [26] sitting at $135°$ and $225°$ in ϕ. On a printed circuit board (PCB), an array of eight plastic scintillators with a silicon photomultiplier (SiPM) readout are placed. For the radiation measurement, this detector provides a fast readout optimized for injection background investigation, i.e. the evolution of injection background relative to the injection cycle. However, it is not sensitive to the position of the incoming charged particles with its $20 \times 20\,\text{mm}^2$ scintillator tiles.

- **PLUME:** The PLUME detector [27] is placed right behind CLAWS at $135°$ and $225°$ in ϕ. On a SiC-foam, $50\,\mu\text{m}$ thick CMOS silicon pixel sensors are placed on both sides of the supporting structure. The very small pixel pitch of $18.4 \times 18.4\,\mu\text{m}^2$ allows a very

precise position measurement of incoming particles. Moreover, the double sided ladders should give information about the impinging direction by using 'tracklets' (hit association on both detector sides). One of the two ladders is slightly tilted at an angle of about 20° in respect to CLAWS for better understanding of the radial distribution of the backgrounds.

2.1 Background radiation

The SuperKEKB accelerator is designed to produce a 40 times higher instantaneous luminosity than the previous KEKB. In addition to the amount of events, the accelerator will produce a much higher background affecting the Belle II detector. The sub-detector closest to the interaction point will be the PXD detector. The total amount of background radiation is unknown because there was no comparable experiment to study this. Therefore, the dose which the PXD and the SVD have to withstand, particularly before the machine is tuned, is unclear. In order to determine a value for the expected background radiation, one uses Monte Carlo techniques to simulate physical processes. In the BEAST II experiment, the simulations should be validated. The backgrounds discussed in this chapter are commonly occurring in the experiment. Therefore, the reasons for background radiation are highlighted in this section, based on references [28],[29].

2.1.1 Luminosity-dependent background

Two-photon radiation (QED): The two-photon QED process contributes the highest amount of background for PXD and dominates all other processes because of its large cross-section. In this process, lepton pairs are produced via the two-photon process, shown in the Feynman diagram in Fig. 2.2. The produced leptons, mainly electron-positron pairs, carry a low momentum.
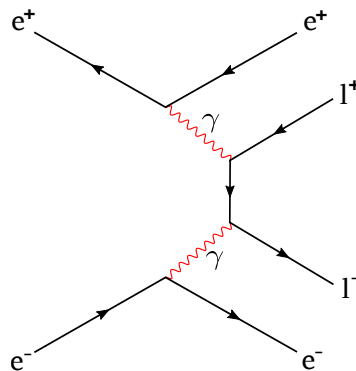
Figure 2.2: Feynman diagram for a two-photon process, producing a lepton pair l^+l^-.

Radiative Bhabha scattering: The second luminosity dependent background is the e^+e^--scattering, also called Radiative Bhabha scattering. In this scattering process, a Bremsstrahlung photon is produced, as shown in Fig. 2.3. The scattered electron and positron travel down the beam pipe away from the IR. Only a small amount can scatter back to the IR after hitting the

beam pipe or magnet.

However, the produced photon collides with the beam pipe or magnet material and is able to excite an atomic nucleus. This process is called giant dipole resonance. In the relaxation of such a heavy nucleus, a single neutron is frequently emitted with a finite probability to hit the PXD. This process is responsible for the largest neutron background and electromagnetic showers for the PXD. It is proportional to the beam current and the vacuum level in the beam pipe. In order to study this process, the beam currents can be varied.
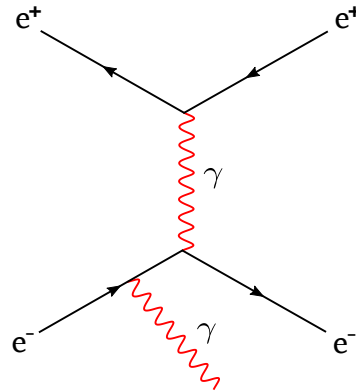
Figure 2.3: Feynman diagram for radiative Bhabha scattering. The generated photon can create a neutron via giant dipole resonance.

2.1.2 Beam-induced background

Touschek effect: The increase of the luminosity is achieved by reducing the transverse size of the bunches without reducing the number of particles. This leads to a higher particle density within the bunch. The Touschek effect describes the Coulomb scattering off the particles inside the bunch which has effects on the beam size and therefore the quality of the beam, also referred to as intrabunch scattering. The change of the direction leads to the escape of the particles from the nominal beam orbit, hitting the beam pipe and magnets. Generated particle showers are able to reach detectors near the interaction region. The Touschek scattering rate is inversely proportional to the square of the beam size $\sigma_{x,y}^2$ and proportional to the number of particles per bunch squared N^2. The scaling dependencies of this effect will increase this background at SuperKEKB because of the nano-beam scheme. Moreover, the Touschek scattering will be higher for the LER compared to the HER (rate $\propto E^{-3}$).

Synchrotron radiation: In a circular accelerator, like SuperKEKB, light charged particles (electrons or positrons) are deflected by magnetic fields. Therefore, the direction of motion changes in the transversal plane, see Fig. 2.4(a).

As a result of the change in the transverse acceleration, a rearrangement of its electric fields is required and the field perturbation which is travelling away from the charge is observed as electromagnetic radiation, called synchrotron radiation. For electrons and the assumption that the bending radius r is constant for all bending magnets, the radiation power for a beam current

I is describes by [30]:

$$P_\gamma = 0.0885 \cdot \frac{E^4 \,[\text{GeV}]}{r \,[\text{m}]} \cdot I \,[\text{A}] \,, \qquad (2.1)$$

with the particle energy *E*. Considering the final conditions, a larger background for HER is expected.

Precautions, e.g. the cone shape of the beam pipes near the interaction region, should prevent the synchrotron radiation from reaching the interaction region. However, the final focusing magnets near the IR, referred to as QCS[1], bend the orbit of the beam and consequently induce synchrotron radiation which reaches the IR and the innermost sub-detectors [3].

In order to reduce the backscattered synchrotron radiation and the fact that the ratio of absorbed to scattered photons goes as $\sim Z^3$, the central part of the beryllium pipe is covered with an additional gold foil (atomic number $Z = 79$) with a thickness of 6.6 μm in the BEAST II experiment.

Beam-gas scattering: Due to inelastic Bremsstrahlung and elastic Coulomb scattering off residual gas, the momentum of beam particles is reduced, resulting in interactions between the particles and the walls of the beam pipe and magnets.

Figure 2.4(b) shows a Feynman diagram for the case of Coulomb scattering. This effect generates particle showers which are one of the major sources of the beam-induced background [3]. The amount of radiation is dependent on the beam current *I*, the vacuum pressure *P* in the ring and the strength of the magnets so that it can be investigated by varying either the gas pressure inside the beam pipe or the beam currents.
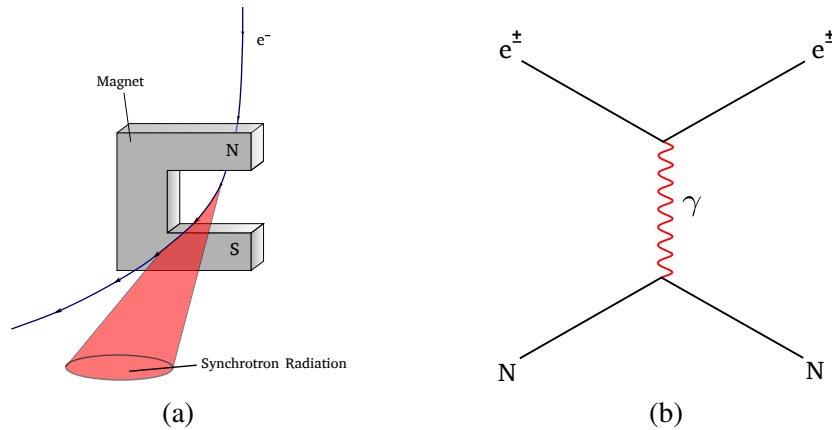
Figure 2.4: (a) Emission of synchrotron radiation. A light particle (electron) is deflected by a magnetic field and emits synchrotron radiation in a narrow cone. (b) Feynman diagram for beam-gas Coulomb scattering. In this process, the particle direction changes due to Coulomb scattering off a nucleus (N) from the residual gas.

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[1] Quadrupole and Compensation Solenoids

2.2 X-ray absorption in silicon

Hybrid pixel detectors with silicon sensors are limited in their detection efficiency by the energy of the particles, the type and the thickness of the sensor material. Using silicon ($Z = 14$), among other particles, photons can be detected. To investigate in which energy range the detector will be sensitive to these photons, a closer look on the attenuation of the γ-quants in the material is needed. The interaction between γ-quants with an intensity I_0 and a material with thickness d is described by the attenuation law:

$$I(d) = I_0 \cdot e^{-\mu d}, \tag{2.2}$$

with the linear attenuation coefficient μ [cm^{-1}] of the absorber material. The coefficient is a function of the energy of the photons hν, the density ρ and the atomic number Z of the absorber material: $\mu = f(h\nu, \rho, Z)$. In order to calculate the absorption probability for photons in the detector sensor, the attenuation coefficient in silicon is taken from `NIST` [31]. The diagram is shown in Fig. 2.5.
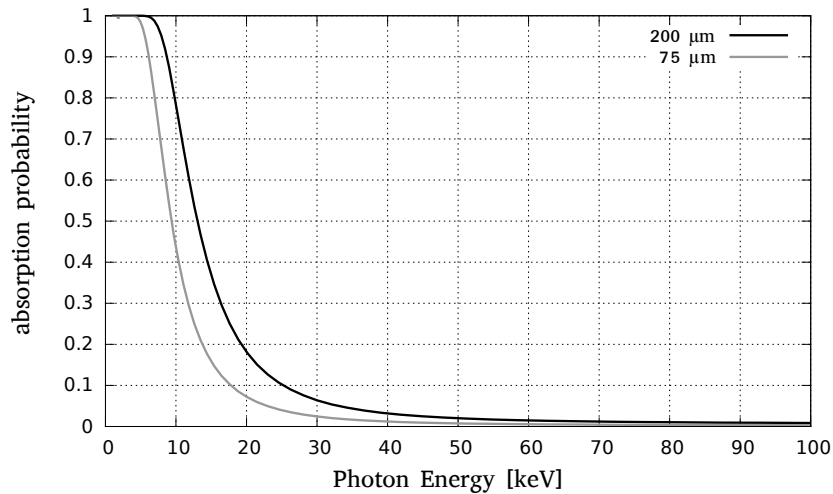
Figure 2.5: Absorption probability for photons in silicon. Comparison of a 200 μm thick sensor (FANGS) and 75 μm sensor (PXD).

The diagram shows the absorption probability for silicon sensors with the sensor depths 75 μm and 200 μm for PXD and FANGS, respectively.
There are two aspects which have to be mentioned in this diagram:

- For higher photon energies, the probability of an interaction with the sensor drops very steep. At 60 keV the probability of an interaction and therefore the detection of this photon is close to zero.

- The probability distribution shows that the silicon sensor of FANGS will absorb nearly twice as many photons as the PXD sensor. Explicitly observed at 10 keV, there is a

probability of 80 % of photon absorption for FANGS and only 40 % for the PXD. Figure 2.6 shows the simulated spectrum of the synchrotron radiation expected for the PXD in the BEAST II experiment.
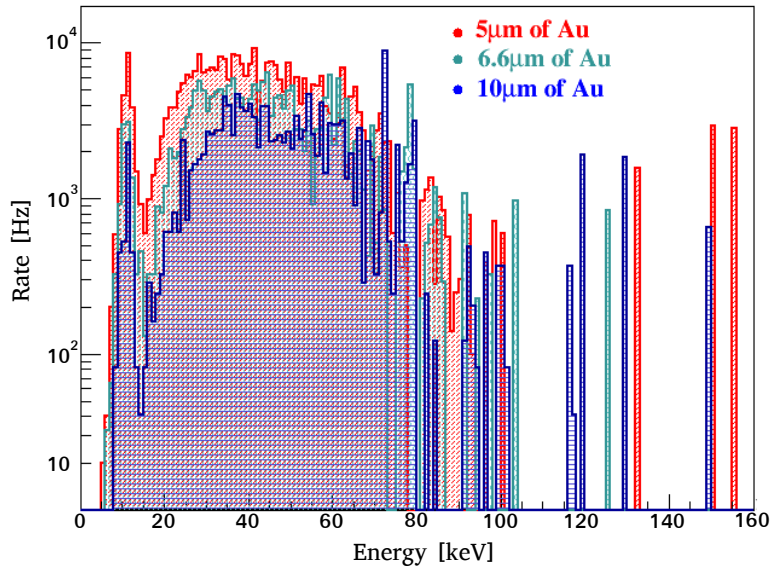
Figure 2.6: Simulated spectrum of synchrotron radiation considering the PXD volume and the thickness of gold (Au) film covering the beam pipe. In the BEAST II experiment, the gold film be 6.6 μm thick [32].

In the diagram, the observed PXD synchrotron radiation rate is simulated with the final geometry and magnetic field configuration of the experiment. Additionally, the simulation is for 75 μm silicon sensors. One has to keep in mind that in Fig. 2.5, the absorption probability for 200 μm sensors is roughly a factor two higher, doubling the rate of synchrotron radiation for FANGS in the energy range from 10 keV to 60 keV.

In the BEAST II experiment, the gold film of the beam pipe will have a thickness of 6.6 μm. Before the installation of the Belle II detector, the thickness will be increased to 10 μm resulting in a better shielding from synchrotron radiation in the final experiment.

FANGS detector

In this chapter, an overview of the FANGS detector, which was assembled throughout this thesis, is presented. The single components of the detector system are described in detail in the following sections. The last section focusses on the test set-up in the laboratory.

3.1 Stave design

The basic units of the FANGS detector system is based on staves like the one in Fig. 3.1. Each stave contains five ATLAS IBL pixel detector modules which consist of the FE-I4 readout chip connected to a $200\,\mu$m thick n-in-n planar silicon sensor. The FE-I4 is designed to withstand a radiation dose up to $300\,$Mrad and a maximum hit rate of $400\,$MHz/cm^2. The commissioning phase of Belle II (BEAST II) will deploy dedicated radiation monitors for beam and background measurements in which the ATLAS pixel detector modules will be ideal for studies under irradiation.

The layout of the stave can be seen in Fig. 3.1, where different regions can be identified:
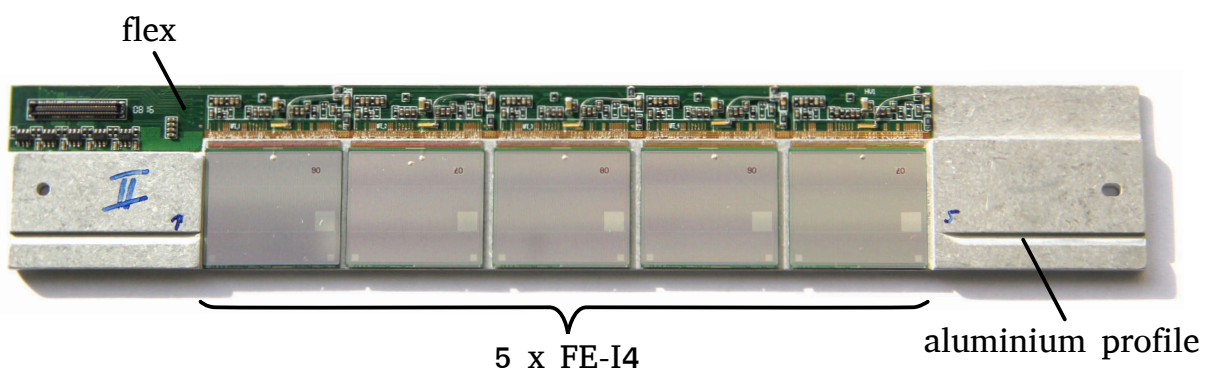
Figure 3.1: Picture of a fully equipped FANGS stave. Five FE-I4 modules are glued on an aluminium profile. The connection with the outside world is done via a flexible printed circuit board (flex).

1. An **aluminium profile** is manufactured with the size of $17.2 \times 2.9\,\text{cm}^2$. Two holes are drilled to attach the FANGS stave on the PXD cooling block with screws. One hole is elongated to avoid tensions due to CTE[1] mismatches. The maximum thickness of the profile is 3 mm at the far right and left of the stave. The central part, on which the five FE-I4 modules are located, is 1 mm thinner. The minimum thickness with 1.5 mm is at the upper part of the stave where the electric supply lines are located.

2. The first step of the composition is the attachment of the flexible printed circuit board, called **flex**, on the aluminium profile using epoxy resin. All signals and currents are transmitted via the flex (see Sec. 3.2). The electric lines are guarded by a kapton layer and connect the exposed gold pads to a 60-pin socket connector. In the ATLAS IBL design, the same electric components are located on top of the sensor. The new flex design provides a higher sensitivity for low keV photons, due to the reduced material budget in front of the sensor. The passive components on the flex are termination resistors and filter capacitors providing data transmissions and the power supply.

3. The heart pieces of this detector system are the five **FE-I4** on each stave, as shown in Fig. 3.2. The glue between the aluminium and the electronics is a thermally conductive silicon gel. This conductive connection is important to dissipate the heat produced by the FE, using the attachment of the profile to the PXD cooling block. The cooling concept is further discussed in Chap. 6.
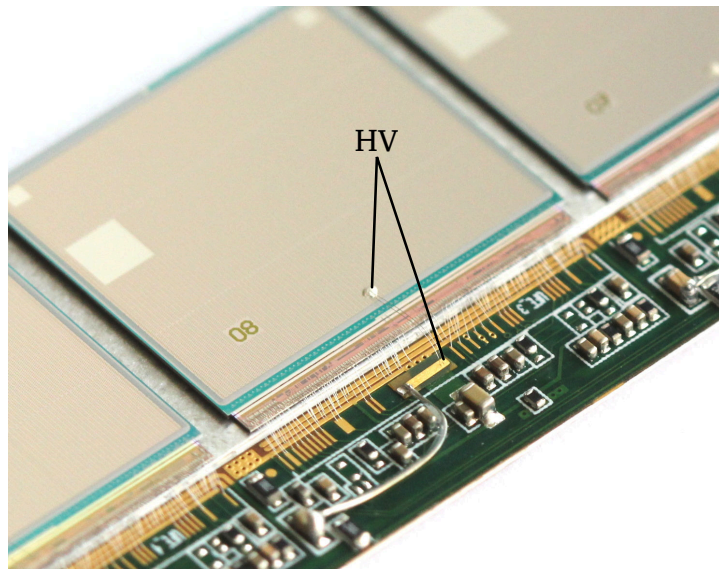
Figure 3.2: Photography of the connection of one FE-I4 to the flex using wire bonds. Additionally, the High Voltage (HV) connection is pictured here.

4. The connection between the five FE-I4 and the flex is done by **wire-bonding**. In this process, on the one side aluminium wires with a diameter of typically 25 μm are attached

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[1] Coefficient of Thermal Expansion

to the gold pads of the flex and on the other side to aluminium pads of the Front-End using ultrasonic welding.

5. In order to operate the detector, the sensor on top of the FE has to be biased with a **HV** to achieve a depletion zone in the silicon bulk. This connection is also shown in Fig. 3.2. The HV line supports all five sensors of the stave in serial. After coupling to a termination resistance and a filter capacitor, the voltage carrying flexible wire is connected to a conductive gold strip positioned between the other bonding pads of the flex. In order to avoid any contact to other electric components, it is stabilized with silicon glue. From the position of the gold strip, two wire-bonds are attached to the sensor.

3.2 Transmissions via flex

In order to propagate ingoing and outgoing signals which are received and transmitted by the FE-I4, the circuit of the flex is used. Figure 3.3 shows the transmission lines between both components, divided into ingoing (upper lines) and outgoing (lower lines) electric support lines. The demonstrated connection is explained in detail below.
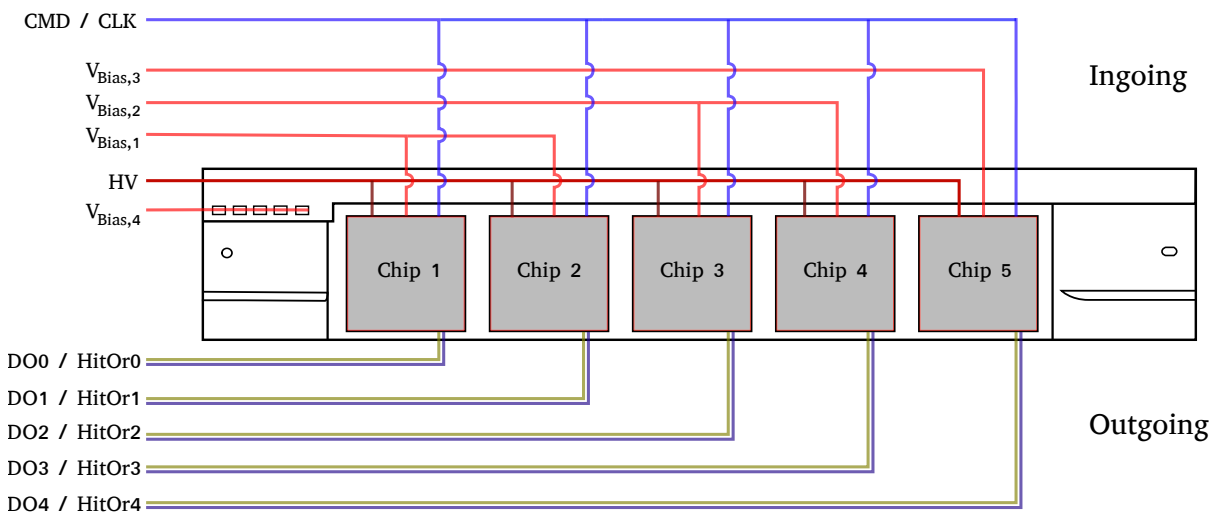
Figure 3.3: Ingoing and outgoing connections between the FE chips and the flex. All electric wires run through the flex.

CMD/CLK: The communication with the FE-I4 chip is achieved by a differential command (CMD) input. In addition, a differential clock (CLK) with $40\,\text{MHz}$ is provided to the FE, sampling the command input on the rising edge of the clock.
As a result of this, each sample is interpreted as a bit and the whole incoming patterns are scanned for valid commands, e.g. local pixel configuration or trigger commands. The lines of CLK and CMD are AC-coupled, which means that capacitors are placed in front of the receiver on each of the differential lines. An AC-couple link guards the data stream against differences

in the ground potential between the receiver in the Front-End and the transmitter in the data acquisition electronics. Otherwise, the data transfer might possibly not work properly due to a given voltage offset in one of the sides. To use this technique, the CMD protocol of the FE-I4 has to be Manchester encoded [33], which requires an implementation in the firmware of the readout. In the encoding protocol, the CMD is sent normally and inverted to fulfill the condition of an equal number of digital zeros and ones, resulting in a speed of 80 MHz. The nominal 40 MHz clock at the receiver side leaves the inverted bits unobserved, and the CMD is thus understood by the FE. The five FE-I4 on the FANGS stave are connected to the same CMD and CLK lines.

$V_{\text{Bias,i}}$: The powering of the FE electronics is accomplished by four bias Voltages ($V_{\text{Bias,i}}$), set to 2.0 V. The first and second two chips share $V_{\text{bias,1}}$ and $V_{\text{Bias,2}}$, respectively. The voltage of the fifth chip is supplied by $V_{\text{Bias,3}}$.

Located on the flex, two low drop-out regulators (LDO) generate the voltage needed by the analog (VDDA = 1.5 V) and digital (VDDD = 1.2 V) part of each FE. The advantage of the LDO is the output of a constant voltage, independent of variations in the input voltage.

If no data connection is provided, each FE-I4 has a current consumption of 20 mA. As soon as the CLK signal is recognized by the chip, the current increases to almost 120 mA. The current consumption is highest in the case of the operation mode in which commands are reaching the FE. The current then is approximately 600 mA.

The voltage supply of 2 V for the five low-voltage differential signalling (LVDS) driver is regulated by $V_{\text{bias,4}}$. The drivers perform a conversion from the single-ended HitOr signal to a differential signal (see Chap. 5).

HV: The HV is applied to the 200 μm thick sensor in order to deplete the silicon bulk from free charges so that electron-hole pairs are generated by passing by ionizing particles. In the circuit of the flex, a single electrical line supplies five sensors with the required voltage of -80 V. Considering Eq. 1.3, the corresponding depletion depth d is given as:

$$d \approx \sqrt{\frac{2 \cdot 11.7 \cdot 8.854 \cdot 10^{-14}\,\text{F/cm}}{1.602 \cdot 10^{-19}\,\text{As} \cdot 2.15 \cdot 10^{12}\,\text{cm}^{-3}} \cdot 80\,\text{V}} \approx 219.36\,\mu\text{m}\,.$$

The applied voltage depletes the entire sensor.

DO/HitOr: The outgoing part of the circuit includes the data (DO) signal as well as the HitOr signal from the FE. Each FE-I4 has its own differential line pair for DO and a single-ended line for the HitOr signal. After the LVDS driver, the HitOr signal is transmitted in a differential wire pair. Both LVDS transmissions use the 8b/10b encoding protocol [34].

The data output rate of 160 Mb/s is achieved by a clock multiplier inside the FE, applied to the nominal 40 MHz clock.

All electric support lines end up at a 60-pin connector socket on the flex. In order to establish a connection between the FE and the back-end electronics, the Intermediate flex is used and presented in the next section.

3.3 The Intermediate flex

The Intermediate flex serves as an interface for the data transmission between the five FE-I4 and the back-end electronics, additionally carrying the cable connection of the power supply. There are two motivations for the necessity of the Intermediate flex: The stave is kept very compact and the accessibility for cable connections is simplified. As soon as the stave is installed and connected to the Intermediate flex, it is used to connect all data and power cables with the data acquisition and power supply systems and provides that all cables are outside the acceptance region.

The layout of the Intermediate flex is subdivided into a flexible and a solid PCB. On top of the flexible PCB, the matching plug of the 60-pin connector is located. On the solid part, there are two `Molex` connectors attached in an angle of 90°. The HV supply and FE-I4 powering is done by 2-pin and 8-pin connectors, respectively.

The Intermediate flex also has a RJ45 connector array, which provides four cable connections between the back-end electronics and the FE. A picture of the Intermediate flex is shown in Fig. 3.4.
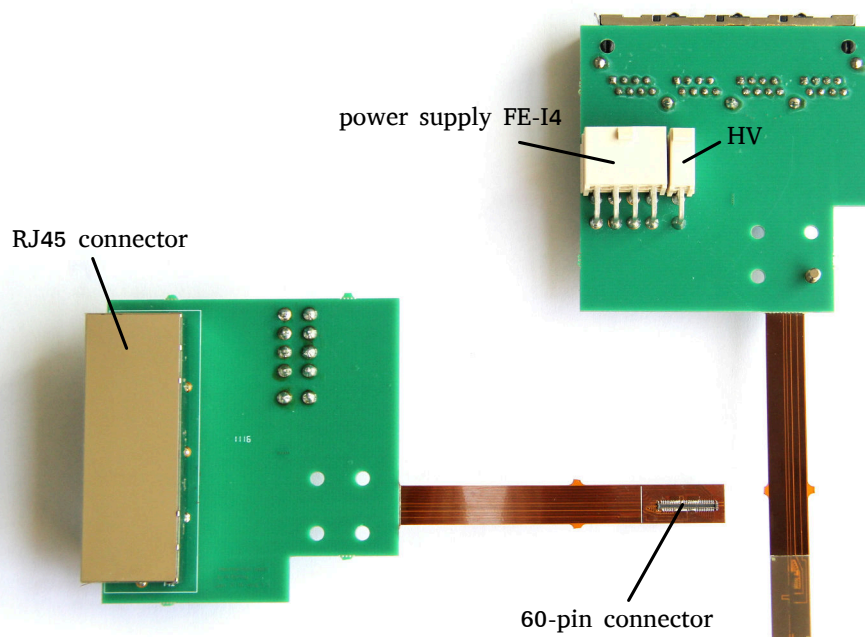
Figure 3.4: Picture of both sides of the Intermediate flex. The `Molex` connectors are used to supply the voltage for the five FE-I4 modules and the sensors (HV). The RJ45 and 60-pin connector for CMD, CLK and data are soldered on the backside.

In order to avoid crosstalk between data and power lines, there are two additional intermediate layers available on the PCB. The data and power circuits are separated from each other within the two inner layers, ending up at the 60-pin connector.

3.4 Chip ID

The five FE-I4 modules on the FANGS stave receive the same CMD due to a differential pair connected to each of the chips. In order to provide multi-chip operation, a chip identification (ID) can be set by using physical connections in form of wire-bonds. Three wire-bonds enable three bits in which an existing connection to the digital voltage (VDDD) means a value of one. In the standard configuration of the wire-bonding, all three wires are set yielding a chip ID of: $111_2 = 7_{10}$. Therefore, the chip ID is set by pulling down different combinations of wires. Using this technique, up to eight different chip IDs are possible. Figure 3.5 shows two different FE-I4 on the FANGS module.
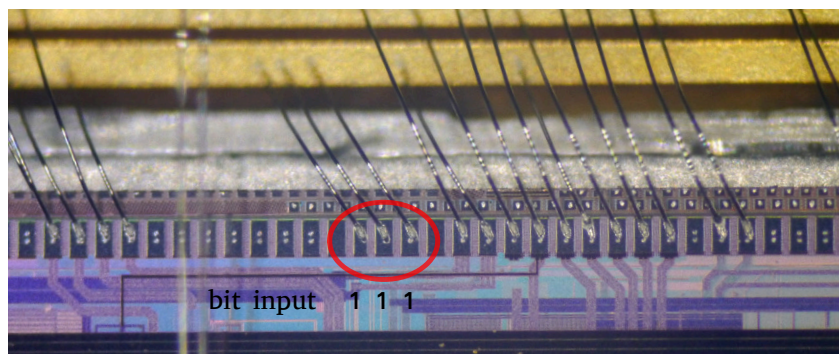
(a) First chip with a chip ID of 7.
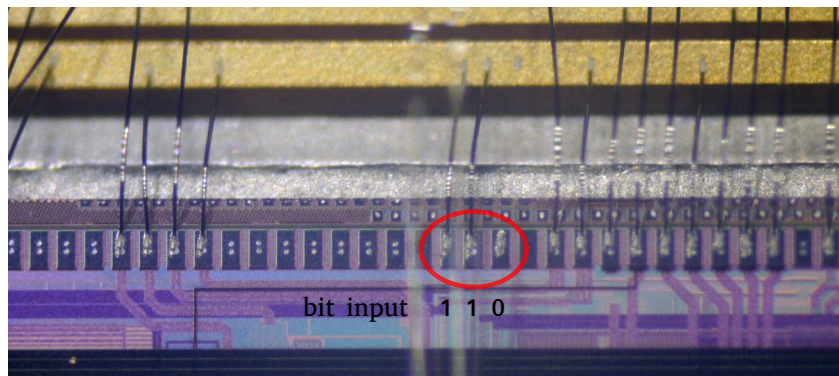
(b) Second chip with a chip ID of 6.

Figure 3.5: Photograph showing the bonding pads of two different FE-I4, taken with the microscope. The wire bonds, which provide the chip ID, are marked with a red circle. (a) All three chip ID wires are set resulting in a chip ID of 7. (b) The last wire bond is pulled down to set the chip ID to 6.

If a chip ID is set, the CMD can be sent to a selected FE chip. In Tab. 3.1, the wire combination as well as the IDs are listed to communicate with the five FE chips.

FE number	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5
Chip ID	$111_2 = 7_{10}$	$110_2 = 6_{10}$	$101_2 = 5_{10}$	$100_2 = 4_{10}$	$011_2 = 3_{10}$

Table 3.1: Listed chip ID for multi-chip operation of five FE chips.

The chip ID numbers have to be implemented in the data acquisition software pyBAR[1], supporting the user interface for communication and analysis of FE-I4 data. The global configuration to have a valid command for the FE-I4 modules of the entire stave is a chip ID of 0.

3.5 Data acquisition - MMC3 Board

In the BEAST II experiment, each FANGS stave will read five FE-I4 in parallel. In order to have a parallel data acquisition (DAQ) and to ensure measurements of timing and angular dependencies of the background radiation, a multi-chip readout is required. The Multi Module Card (MMC3), depicted in Fig. 3.6, is designed by the University of Bonn and allows the communication as well as the readout of five FE-I4 in parallel.
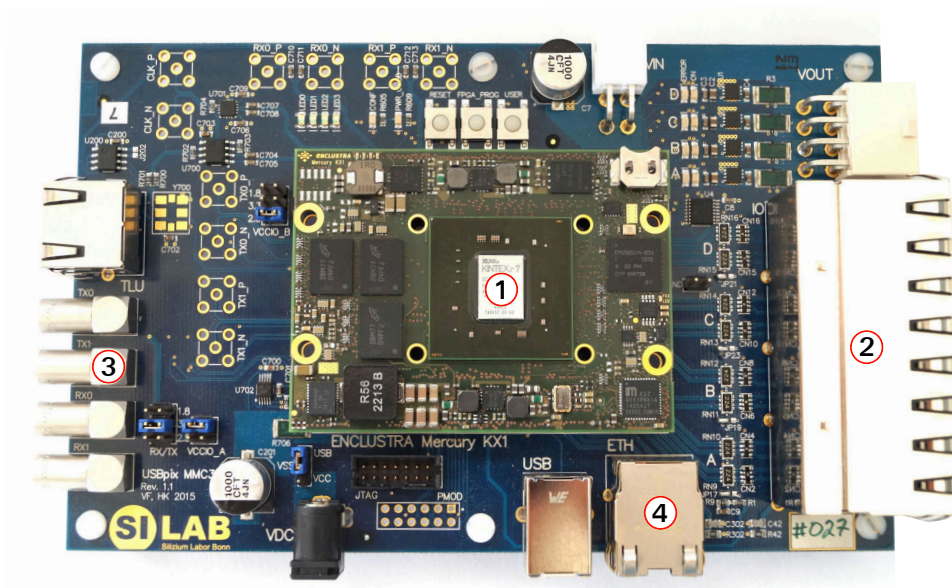
Figure 3.6: The MMC3 board with the Kintex-7 FPGA module (1), eight RJ45 connectors (2) and four LEMO connectors (3). A connection to the PC is implemented via Ethernet (4).

The MMC3 is an upgrade of the MIO[2] board [35] in which an additional FE-I4 adapter card is no longer needed. Furthermore, a readout via USB 3.0 or Gigabit Ethernet is implemented.

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[1] Bonn ATLAS Readout in Python and C++
[2] Multi Input / Output

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The power supply is provided by a constant voltage of 5 V. The multi-chip support is accomplished by a RJ45 connector, providing eight sockets. Therefore, a direct connection of up to eight FE-I4 modules is achieved. Additionally, four LEMO connectors can be used for ingoing and outgoing data transfer. The structure of the board is divided into two parts: The basis of this system is a custom-made carrier board which is attached to an `Enclustra` Mercury KX-1 module via two 168 pin connectors. The centrepiece is based on a commercial FPGA module, shown in Fig. 3.7. The `Xilinx` Kintex-7 FPGA provides the logical and sequential functionality of the readout board with 158 input / output-blocks. The firmware, written in Verilog HDL[1], configures the FPGA and provides functions for data handling and the communication to the FE-I4. The firmware is sent via JTAG[2]. Moreover, data can be stored in a flash memory to extend the internal FPGA memory. In order to describe the working principle of the firmware functions, called modules, Fig. 3.8 shows

Figure 3.7: Mercury KX1 module with the Kintex-7 FPGA on top.

the summarized blocks for communication with the PC, handling and storing data sent by the FE chips. The individual modules are described below.
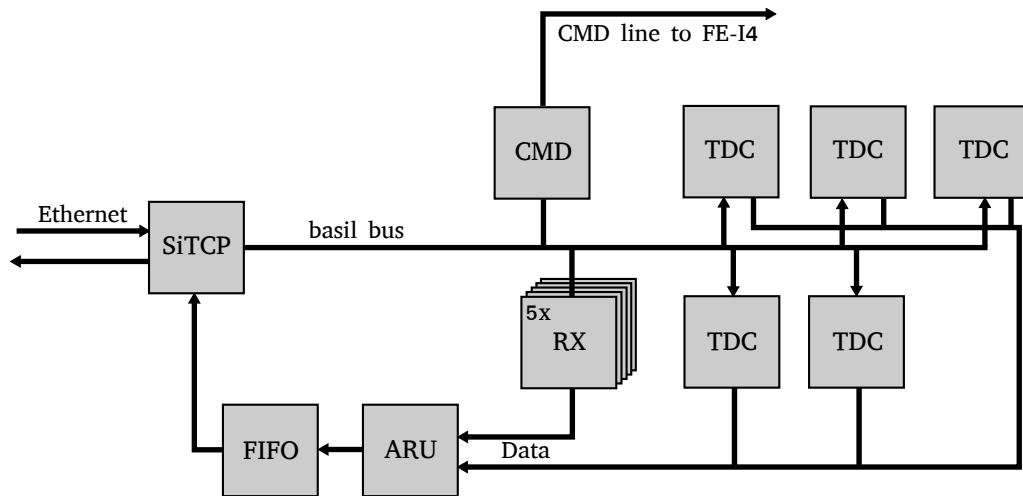
Figure 3.8: Schematic of the module arrangement in the FPGA firmware.

- SiTCP (Silicon Transmission Control Protocol): The SiTCP allows a direct connection between the FPGA and the PC via Ethernet. Furthermore, it is possible to receive and transmit data at the same time due to the pipeline-based circuits design [36].

- Basil bus: Basil is a modular readout framework providing a simple and fast DAQ. It supports different hardware components, FPGA firmware modules and control software

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[1] Hardware Description Language
[2] Joint Test Action Group: interface for programming and debugging of a micro controller

based on python. The framework is used to access the readout hardware as well as connecting all control and data taking modules via the basil bus.

- CMD module (Command): The CMD generates the FE-I4 commands using a data stream and clock.

- TDC module (Time to Digital Converter): The TDC module digitizes the input pulse and sample the ToT, using the FPGA 640 MHz.

- RX module (Receiver): The RX is the FE-I4 data receiver which allows continuous data recording from the chips while monitoring errors and synchronizing the data taking phase with the CLK.

- ARU (Arbiter Unit): The ARU is placed in front of the FIFO to select data streams using the round-robin algorithm. The algorithm provides the data handling of all processes in a circular order and the access to the memory for an equal share of time.

- FIFO (First-In-First-Out): The FIFO is a memory, where the oldest entry (first-in), is processed first in the queue. Data from the RX and TDC is stored in the FIFO with the ability of a continuous readout via Ethernet.

The received data words from the FE-I4 have a length of 32 bit. Since five FE are used in parallel, the data from different chips is identified by source coding ID bits within the 32 bit data words.

3.5.1 Data format

The continuous data acquisition without interrupts and preserving all information require a data format to store all the information sent by each Front-End. Therefore, words with 32 bit lengths are used to deposit the information, e.g. timestamps, ToT values and pixel position of the recorded hit.

In order to use five FE sending data at the same time, an additional unique identification is required. For this reason, the following data format has been implemented. Data words sent by the FANGS detector have the data format:

Trigger words: 1$\underbrace{\text{xxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx}}_{\text{31 bit trigger data word}}$

TDC words: 0$\underbrace{\text{yyy}}_{\text{3 bit ID}}$ $\underbrace{\text{xxxx xxxx xxxx xxxx xxxx xxxx xxxx}}_{\text{28 bit TDC data word}}$

FE words: 0000 $\underbrace{\text{yyyy}}_{\text{4 bit ID}}$ $\underbrace{\text{xxxx xxxx xxxx xxxx xxxx xxxx}}_{\text{24 bit FE data word}}$

The data separation is carried out by implementing IDs in the beginning of a word, referred to as data header. The data header (y) includes the ID and thus the origin of the word followed by the data (x), including the deposited information. The received raw data for each readout cycle

always starts with a trigger word. Subsequently, the TDC word is recorded with the charge information of the pixel carrying the highest charge. The recorded FE words originate from all pixels with charge above the discriminator threshold.

In order to separate the data, a splitter is implemented. The splitter distinguishes between the ID bits (y) of the 32 bit words, represented in Tab. 3.2.

FE number	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5
TDC/FE ID	0001	0010	0011	0100	0101

Table 3.2: Identification numbers for the five FE-I4s on a single FANGS stave.

The presented concept is implemented in the FPGA firmware for FANGS to support the multi-chip readout for five chips in parallel.

3.5.2 Triggered data readout

Charge information and corresponding time stamps from the pixels are stored in buffers. In order to read out the stored information from these buffers, a trigger has to be transmitted. Charges which reach the analog part of the pixel cell simultaneously activate a trigger latency counter. From a programmed trigger latency, it counts down in units of 25 ns (based on the revolution time between colliding bunches at the LHC[1]).

During the time the latency counter counts down to the trigger latency, the analog pixel cell is not able to record any further incoming charge. If the Front-End receives a trigger, the hit data is transmitted in the form of a FE word from the buffers to the end of chip logic.

The maximum latency can be set between 0 and 255 clock cycles. The FE-I4 modules in the FANGS detector are set to the optimal value for the cable length of 28 m, resulting in a storage time for an event of: $218 \cdot 0.025\,\mu s = 5.45\,\mu s$. Thereafter, the buffer and counter are deallocated again. However, if no trigger signal is received the buffers and counter are deallocated and the charge information is deleted.

The FE chips used in FANGS will be sensitive to the internal trigger and additionally to an external one.

Internal trigger

Each comparator output of the pixel cells can be connected to a HitOr bus, using a logical OR. Whenever one of the enabled pixel comparators is active high, the HitOr signal is high. Therefore, a trigger word is sent to the FPGA on the MMC3 board. This trigger causes a subsequent CMD to be sent from the FPGA to the FE.

Having five FE-I4 on the FANGS stave, it is implemented in the FPGA firmware to trigger only on a received HitOr signal of a certain FE or an arrangement of devices. The configuration (`TRIGGER_SELECT`) is embedded in the readout software and is given in Tab. 3.3.

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[1] Large Hadron Collider near Geneva, Switzerland, where the ATLAS detector is operated.

FE number	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	All
Trigger selection	1	2	4	8	16	31

Table 3.3: Input to select the trigger for all five devices.

In order to activate the readout at all incoming HitOr signals, one has to take the sum of the selection numbers, i.e. the selection number to trigger with five FE-I4 has to be 31. With the sum of the selection numbers, it is also possible to trigger using certain FE-I4 on the FANGS stave.

External trigger

The second application for triggering the data acquisition is the trigger provided by an external system, e.g. from the accelerator or Belle II detector. This type of an external trigger can support variable trigger frequencies and support the synchronization of different detector types in the BEAST II experiment by using for example the frequency of bunches crossing the detector or injected bunches in the accelerator. The signals can be induced via the LEMO connectors, connecting the signal generation side with the FPGA on the MMC3 board. The input has to be a rectangular pulse to simulate a HitOr signal, e.g. with a pulse height of 2 V and a width of 200 ns. Receiving the signal from the pulse generator, the FPGA transmits the trigger signal to the FE, causing the subsequent readout.

3.6 Laboratory test set-up

Throughout this thesis, the measurements and tests of the FANGS stave are carried out with final components in order to test the FANGS stave's applicability under realistic conditions. In the BEAST II experiment, the distance between the detector and the back-end electronics will amount to 28 m with one intermediate patch panel. Figure 3.9 shows the conditions for cable routing of a single stave.
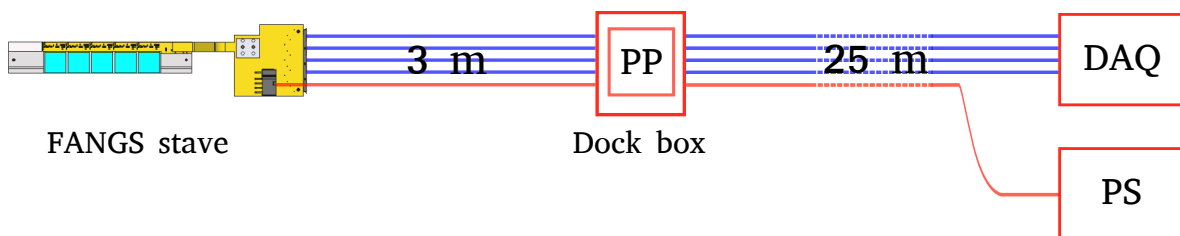
Figure 3.9: Schematic of the distances between the components of a single FANGS stave in the BEAST II experiment. The cables are routed 3 m to the patch panel (PP) located in a Dock box. From there, cables are routed over 25 m to the back-end electronics and the power supply (PS).

From the detector at the interaction region, data and power cables are routed over 3 m to a docking box located in the backward region of the detector. In the experiment, it is not allowed to have direct coupling between detectors and the DAQ/PS. Therefore, a patch panel was designed to establish an intermediate connection point between both components. Finally, there are 25 m from the patch panel to the MMC3 board. The test set-up is mimicking the final experiment and shown in Fig. 3.10.
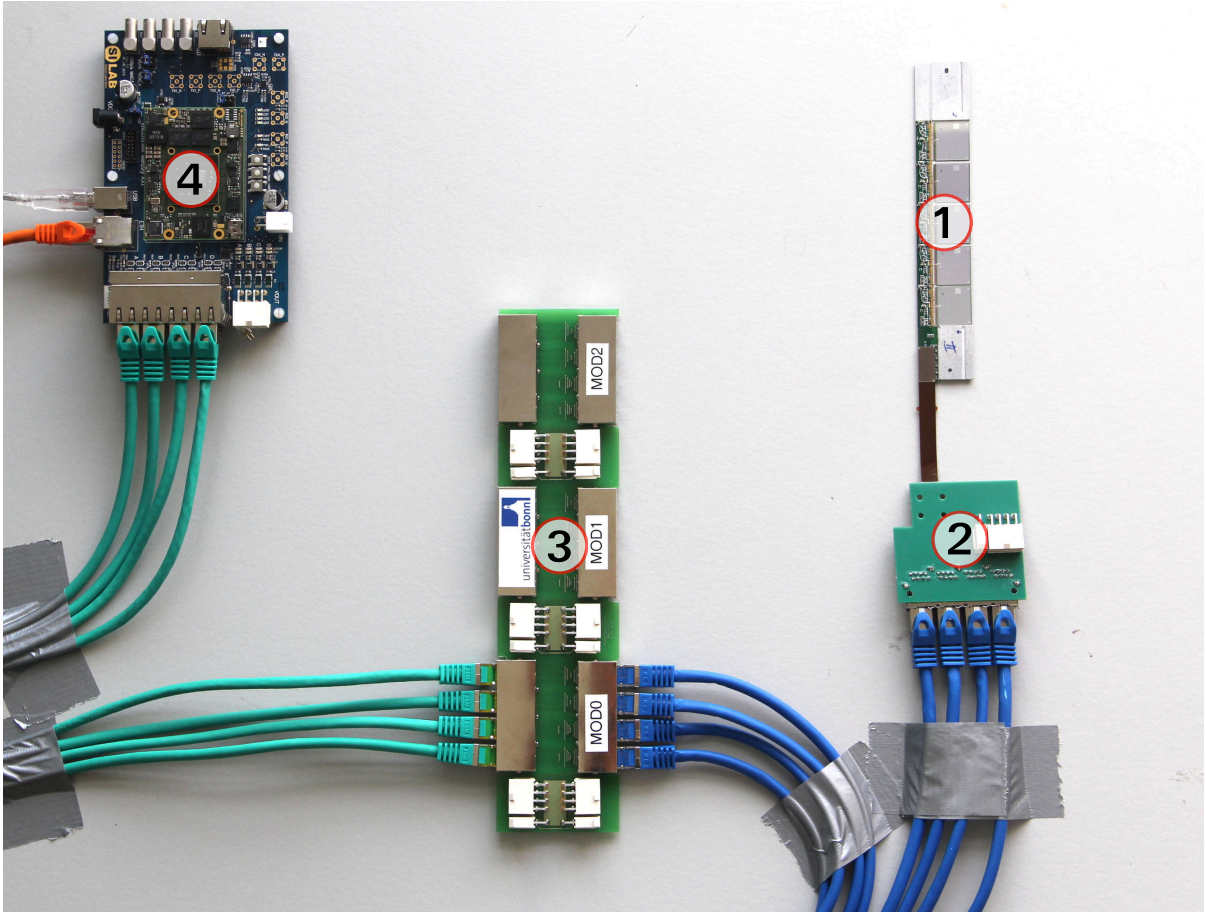
Figure 3.10: Layout of the test set-up in the laboratory. It consists of a single FANGS stave (1), connected to the Intermediate flex (2). From there, the cables are routed over 3 m to the patch panel (3). Four 25 m cables provide the signal propagation to the MMC3 board (4). Cables for power supply are not illustrated in this picture.

The measurements in the next chapters were carried out with all components shown in the test set-up. In addition, a cooling block was attached on the backside of the stave providing a constant temperature of 15 °C at the profile.

Characterization of the FANGS stave

This chapter focusses on the measurements performed with the FE-I4 on the FANGS stave. In the first part, the tuning procedure of the FE as well as the HitOr calibration are described. The second part deals with system calibration and performance, using radioactive sources. By analysing energy spectra, the calibration of the PlsrDAC is carried out.

4.1 FE-I4 tuning

The constituents of the FE-I4, explicitly transistors in the amplifiers and discriminator, always show variations in the production stage, resulting in a different response to an injected charge, e.g. varying ToT, as shown in Fig. 4.1. Therefore, the charge information is not accurately reconstructed and a tuning of the feedback currents and the discriminator threshold for every pixel of the entire matrix is mandatory before any operation at the experiment.
The iterative process of tuning is divided into two parts: The tuning of the global matrix and on pixel level.
The global tuning of the discriminator threshold and the preamplifier feedback current are carried out before the tuning on pixel level with the use of TDAC for the threshold and FDAC for the feedback current (see Fig. 1.7). The tuning algorithm includes the following parameters to adjust the FE-I4 performance:

- Target threshold: The target threshold of the discriminator in units of PlsrDAC sets up the lowest charge that can be recorded from the FE-I4.

- Target charge: The charge in units of PlsrDAC which the tuning is targeted to by the algorithm.

- Target ToT: The target ToT value of the corresponding target charge. This value is responsible for the limits of the recorded charge range. Consequently, the dynamic range can be accommodated to the expected energy range.

- Global / Local iterations: These two values define how often the global and local threshold / feedback current tuning are looped.

After completing the tuning, the charge injections are performed, using the internal circuit of the analog pixel cell. To demonstrate the result, the recorded ToT distribution of a tuned FE-I4 is shown in Fig. 4.2. The chip is tuned to a target charge value of 280 PlsrDAC with a resulting target ToT of 8. The injection procedure is repeated one hundred times and the ToT value is recorded.
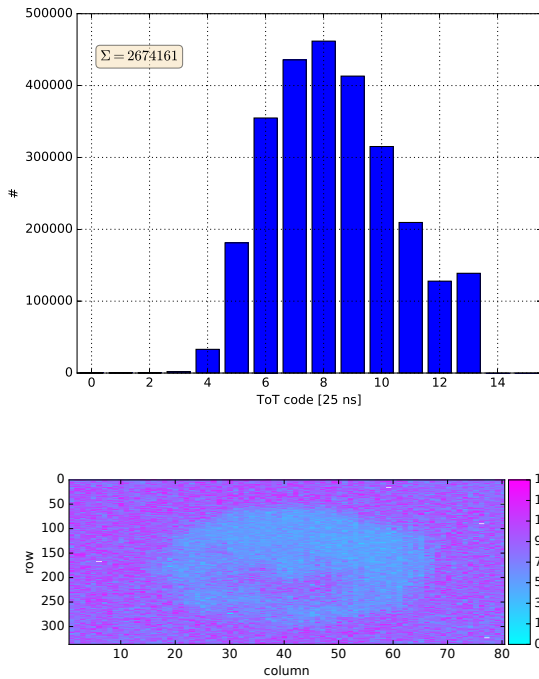
Figure 4.1: ToT (in units of 25 ns) distribution of an un-tuned FE-I4 for an internal injection of 280 PlsrDAC (upper plot). ToT map for the entire matrix (lower plot).
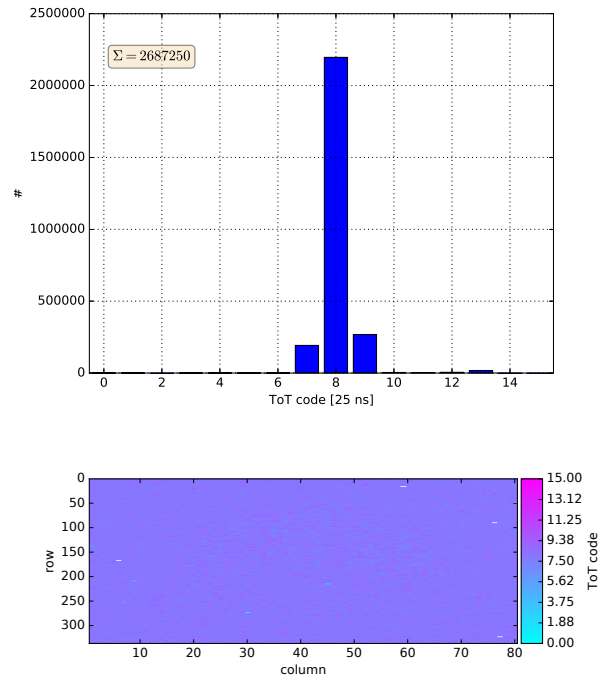
Figure 4.2: ToT (in units of 25 ns) distribution of a tuned FE-I4 for an internal injection of 280 PlsrDAC (upper plot). ToT map for the entire matrix (lower plot).

After the tuning, the majority of the analog pixel cells in the matrix responds with a ToT of 8 for an injected charge of 280 PlsrDAC, showing an improvement for the entire matrix. Despite the tuning, there is no completely uniform ToT response observable. This underlines the variations of the analog pixel cells. For this reason, the HitOr calibration is carried out.

4.2 HitOr calibration

The transfer from injected charge to ToT may slightly differ for each pixel on the matrix even after the performed tuning, as it is seen in Fig. 4.2. An additional calibration is required, referred to as HitOr calibration. In this calibration, charges are repeatedly injected and the ToT and TDC values are recorded for each pixel. The outcome is a table of reference values, describing how the ToT and TDC values respond to altered injection charges.

Figure 4.3 shows the behaviour for a single pixel of both methods in a range of 30 - 800 PlsrDAC

in steps of 1 PlsrDAC. For each step, the injection is repeated for two hundred times. The values and errors originate from the mean and standard deviation, respectively.
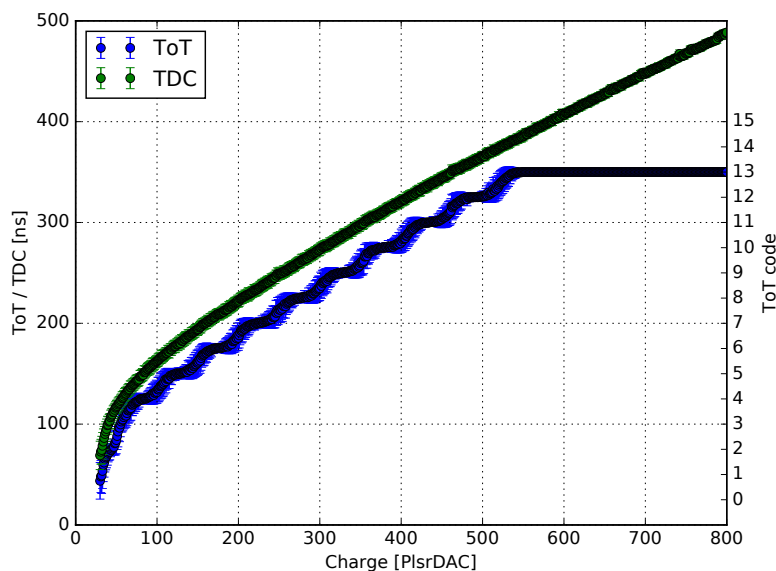
Figure 4.3: A HitOr calibration for a single pixel with ToT and TDC values as a function of the injected charge. The corresponding ToT code is shown on the secondary y-axis.

The measurement shows the steps and a saturation of the ToT distribution at 520 PlsrDAC caused by the use of the 40 MHz clock in the ToT determination. Compared to the ToT signal, the TDC method improves the resolution in the chosen energy range. However, the TDC method only provides the discriminator readout of the highest charge carrying pixel. This method is used in the next section to perform scans of radioactive sources.

4.3 PlsrDAC calibration using radioactive sources

Within the BEAST II experiment, the TDC method is used to measure the energy spectrum of the background radiation. In this method, the HitOr output is sampled with the faster 640 MHz clock, provided by the FPGA located on the readout board. Therefore, the smallest time resolution is 1.563 ns (compared to 25 ns for ToT method). The charge reconstruction performance can be accessed by illuminating the detector with a radioactive source of known type and energy. The used source is Americium-241 (^{241}Am), whose dominant γ-peak is at an energy of 59.54 keV ($\gamma_{2,0}$) and an secondary peak at 26.34 keV ($\gamma_{2,1}$) [37].

The performed source scan records the hits from the radioactive source generating trigger signals by the HitOr of the FE-I4. Three significant tests for the FANGS stave are carried out with this measurement:

- The functionality of the FE module

- Charge collection in the sensor

- The processing of the data in the FE including the transmission to the readout board.

Before each measurement, the chips are tuned and calibrated and an array of pixel is selected to execute the measurement. Figure 4.4 shows the recorded TDC spectrum of an [241]Am source.
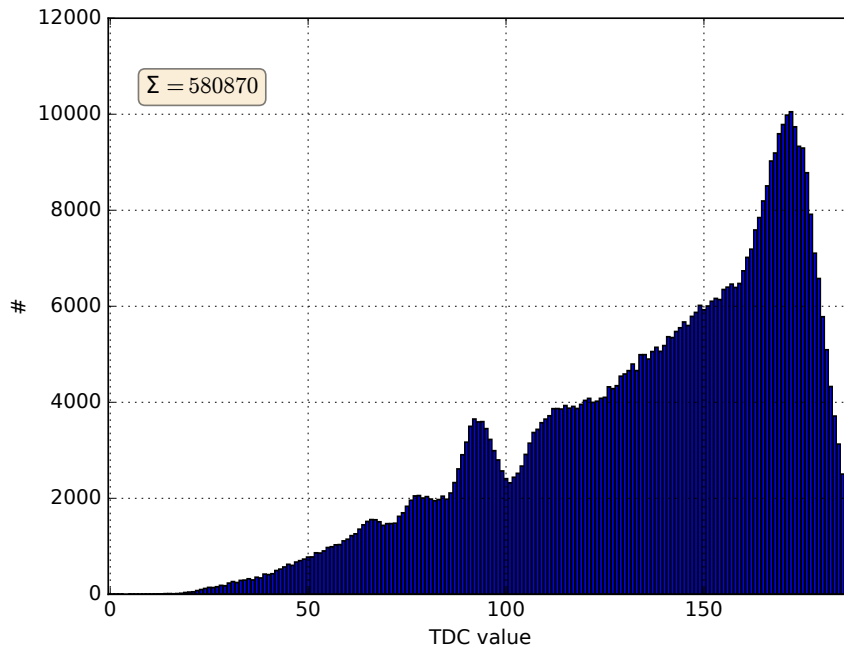
Figure 4.4: TDC spectrum of [241]Am measured with the FE-I4 on the FANGS stave without cuts.

Due to the fact that the TDC collects the data from the HitOr, the measurement consequently shows the spectrum of the illuminated pixel with the highest charge in units of TDC values. The processed data of the selected pixel area is combined and averaged.
Using the HitOr calibration, the TDC values for the used pixel array can be determined to a corresponding charge value in units of PlsrDAC.
If more than one pixel is fired, only a fraction of the energy is deposited on the pixel and thus the charge information of the actual hit is distorted. Therefore, additional criteria for the hit selection are applied to the recorded data, i.e. the number of clusters as well as the cluster size is set to one. Since the TDC method is a single pixel analysis, the resolution can decrease without these cuts. In Fig. 4.5, the [241]Am gamma spectrum is shown after the conversion from TDC values to PlsrDAC including the discussed cuts.
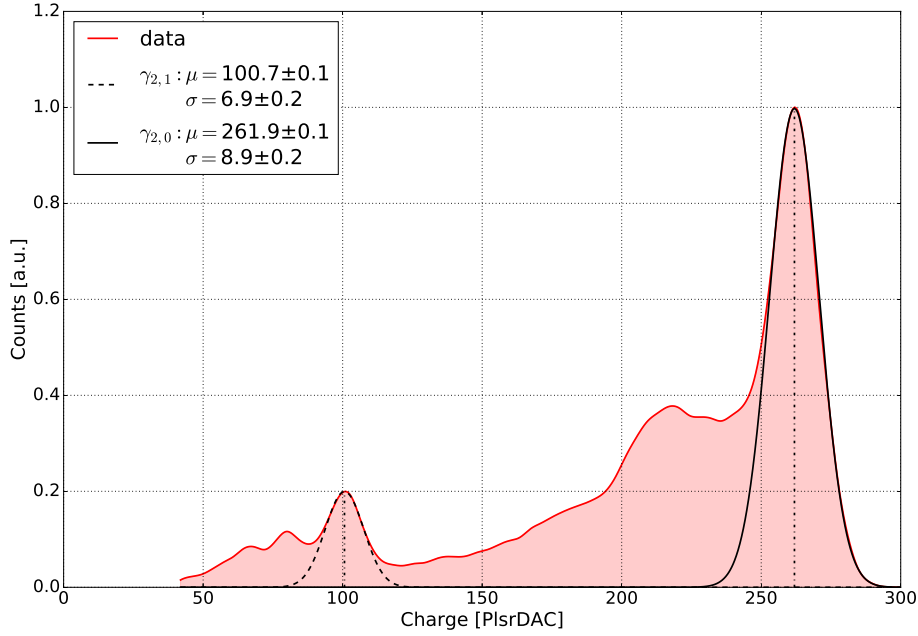
Figure 4.5: Recorded ^{241}Am gamma spectrum measured with the FE-I4 on the FANGS stave, using single pixel clusters. The gamma peak positions are reconstructed with two Gaussian fits.

In the ^{241}Am spectrum, two Gaussian distributions are fitted to the recorded data in order to extract the peak positions. The Gaussian function is described by:

$$f_{\text{Gauss}}(x) = A \cdot \exp\left(\frac{-(x-\mu)^2}{2\sigma^2}\right). \tag{4.1}$$

The extracted peak position of gamma transitions $\gamma_{2,1}$ and $\gamma_{2,0}$ are $(100 \pm 6)\,\text{PlsrDAC}$ and $(261 \pm 8)\,\text{PlsrDAC}$, respectively.

In order to determine the deposited energy in units of eV, the PlsrDAC calibration is performed. In the calibration procedure, radioactive sources with known gamma transitions are used to generate a correlation between PlsrDAC and the deposited energy. Because of the HitOr calibration and the conversion from TDC values to PlsrDAC, this correlation has to be linear. Additional inaccuracies arising on pixel level of the FE-I4 consequently require the individual calibration of each chip used for FANGS prior to the experiment.

The conversion is established by plotting the extracted peak position in units of PlsrDAC against the literature value of the respective peak in units of keV. In order to have at least three points for the calibration, a variable Americium source with a Terbium-56 (^{56}Tb) absorber is used. The measured gamma peak of the ^{56}Tb K_α transition with an energy of 44.23 keV is shown in Fig. 4.6. The extracted peak positions as a function of the literature values are shown in Fig. 4.7.
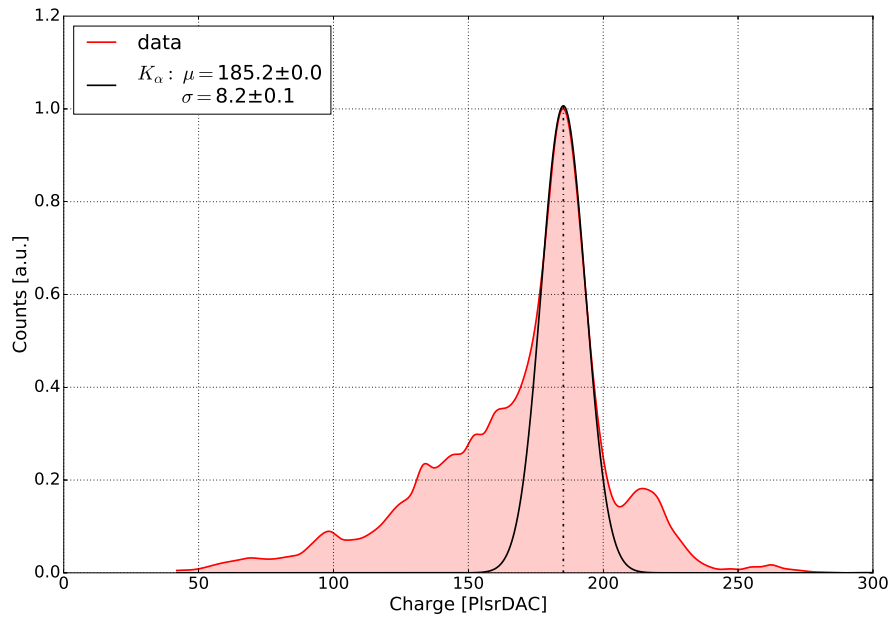
Figure 4.6: Recorded ^{56}Tb gamma spectrum measured with the FE-I4 on the FANGS stave, using single pixel clusters. The gamma peak position is fitted with a Gaussian function. In addition, the K_β transition can be observed on the right side.
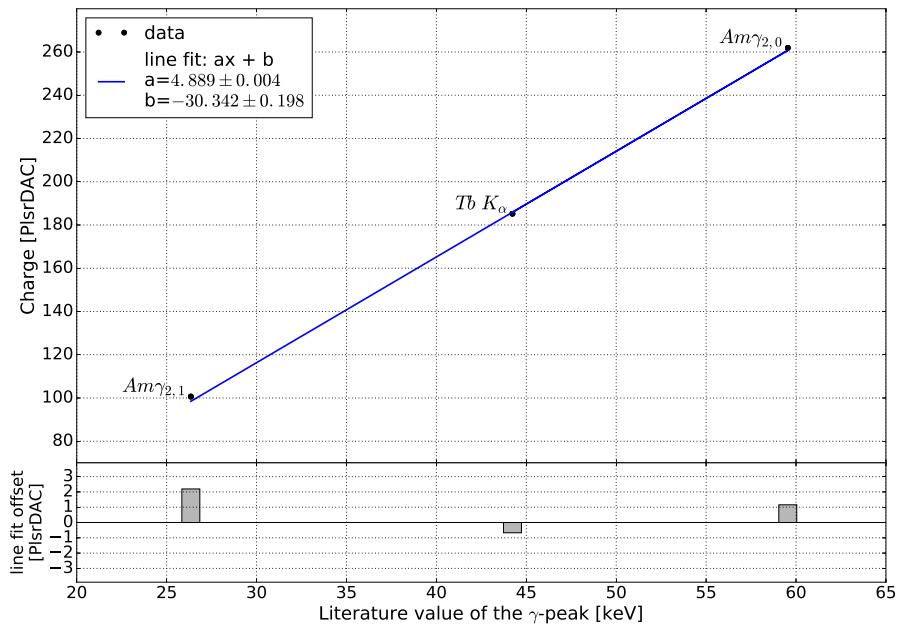
Figure 4.7: PlsrDAC calibration using the extracted peak values from the source scans. The bars in the lower part indicate the distance of the value to the line fit.

The straight line fit, using the linear function $y = a \cdot x + b$ with the slope a and offset b, yields to:

$$y = (4.889 \pm 0.004) \, \text{PlsrDAC/keV} \cdot x + (-30.342 \pm 0.198) \, \text{PlsrDAC}. \tag{4.2}$$

As a result, the function can be used as a transfer function to convert from PlsrDAC to keV.

The validity of the transfer function can be determined by using an additional radioactive source. The variable Americium source is used again with a Barium-133 (^{133}Ba) absorber. The recorded spectrum of the excited ^{133}Ba is shown in Fig. 4.8 after the conversion using the transfer function.
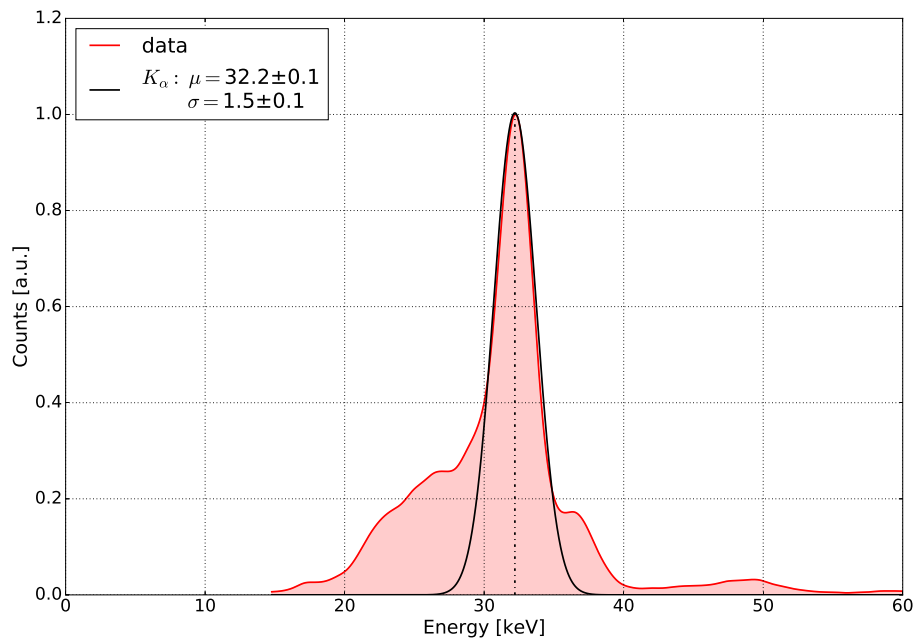
Figure 4.8: Calibrated gamma spectrum of excited ^{133}Ba recorded with the FE-I4 on the FANGS stave, using single pixel clusters. The K_α transition is fitted with a Gaussian function.

The recorded peak of (127.0 ± 0.6) PlsrDAC is converted into energy by using Eq. 4.2:

$$E_{K_\alpha} = (32.18 \pm 0.13) \, \text{keV}.$$

The uncertainty is determined by using Gaussian error propagation. Considering the error limits, the measured value is in agreement with the expected value of 32.06 keV. Therefore, the conversion from PlsrDAC to keV is validated and can be used for the final experiment.
Throughout this chapter, the occurring fluctuations of the performance observed within one FE-I4 is due to variations of different chips. In order to achieve the best energy resolution, the transfer functions are determined for each FE-I4 on the first FANGS stave, listed in Tab. 4.1. The related diagrams can be found in App. A.

	slope $\mathbf{a}$ / PlsrDAC/keV	offset $\mathbf{b}$ / PlsrDAC
Chip1	(4.889 ± 0.004)	(-30.342 ± 0.198)
Chip2	(4.568 ± 0.005)	(-23.883 ± 0.237)
Chip3	(4.074 ± 0.007)	(-14.763 ± 0.289)
Chip4	(4.389 ± 0.017)	(-27.565 ± 1.012)
Chip5	(4.599 ± 0.001)	(-22.474 ± 0.044)

Table 4.1: Slope and offset of the transfer function for each FE on the first FANGS stave. The function can be used to convert from PlsrDAC to keV in the final experiment.

The measurements show that the FE-I4, as well as the sensors are able to reconstruct the deposited charge of the photons. For the BEAST II experiment, the transfer function can be used to determine the energy range of the recorded background radiation.

Irradiation campaign

The data transmission from the detector to the back-end electronics is an important task for all presently available detectors because of the occurring distance between the point of data taking and data processing. The signals are transferred over several meters of cable. The FANGS modules will be set in 28 m distance to the DAQ system.

In order to avoid signal losses and to maintain signal quality, data is sent over LVDS links between the FE-I4 and the electronics. Since the HitOr signal is single-ended, the signal of the five FE-I4 is routed to an equal number of dual inverter gates (LVDS driver) located on the flex. In Fig. 5.1, the position as well as a magnification of the dual inverter is presented.
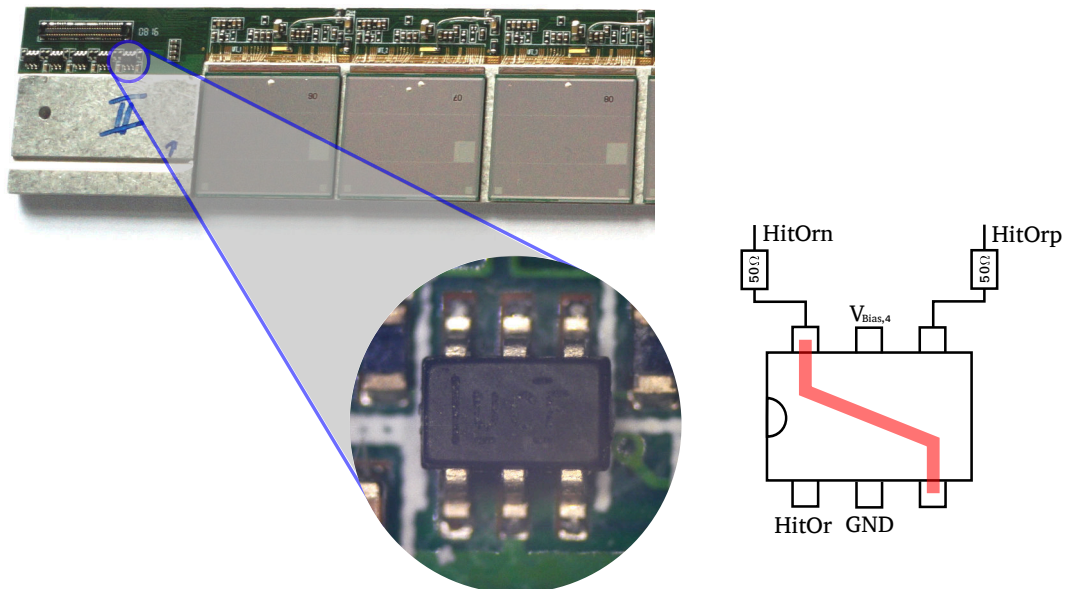
Figure 5.1: Position of the LVDS driver on the flex. The magnified picture shows the integrated circuit (IC). On the right side, the input and output of the IC is shown. The single-ended HitOr signal is inverted on the one hand and redirected to the second input on the other hand, resulting in a differential signal HitOrp and HitOrn. The IC is supplied by $V_{Bias,4}$ (see Fig. 3.3).

The working principle of LVDS is to create a differential signal with a low-voltage amplitude, using a constant current source. Based on the study of differential HitOr signals propagating over 30 m of cable, which showed no influence on signal integrity [21], the LVDS technique is implemented. It is a method which is widely used for high-speed data transfers and additional information on this technique can be found in detail in [38].

The driver is a small integrated circuit (IC), based on two inverters in which the output of the first inverter is connected to the input of the second inverter resulting in a differential signal.

In the BEAST II experiment, the electric components will be exposed to the existing radiation during their lifetime. The occurring effects on the FE-I4 and the sensor have already been confirmed [39]. Since the driver is manufactured for industrial purposes, the impact of radiation on the performance of the components has to be investigated, or more precisely on the CMOS[1] transistors within the dual inverter. One of the main effects in these transistors is the generation of electron-hole pairs in the SiO_2 gate oxide due to ionizing particles [40]. The induced electrons and holes are moving in the SiO_2 and only a fraction of them will recombine. However, the electrons have a higher mobility than the holes and are swept out of the isolator. Consequently, the holes either remain in the place of creation or are transported to the interface of the gate oxide and the doped silicon of the transistor. Here, the holes are trapped. Both effects cause a shift of the threshold voltage in the MOS transistor, inducing a change of the needed voltage to turn on the transistor.

Considering these effects of radiation damage, a detailed investigation on the radiation hardness of the electrical component is conducted in this chapter.

In order to investigate the behaviour of the LVDS driver, the component has been irradiated at the Irradiation Center at the Karlsruhe Institute of Technology (KIT), using a X-ray tube. The behaviour of two main characteristics was investigated:

- The behaviour of the power consumption of the driver. The effect of a threshold shift should increase the current consumption and can end up in a breakdown of the driver.

- The signal integrity and quality of the HitOr signal. The signal is measured at the Intermediate flex and at the back-end electronics. In between, the signal will propagate 3 m to the patch panel and from this point additional 25 m to the MMC3 board.

In the course of this work, the total ionizing dose (TID) was set to 4 Mrad, which is more than the expected value for FANGS in the period of the experiment based on extrapolations from the previous BEAST experiment [41]. Due to the shielding effect of the PXD cooling block from the particles that come from the IR, the LVDS driver will receive an even smaller dose. Nevertheless, the performance is tested to this value.

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[1] Combination of an NMOS and PMOS transistor.

5.1 Current consumption and signal integrity

During the irradiation campaign, the main goal was to investigate the radiation influence on the LVDS drivers. For this reason, the LVDS driver of one blank FE-I4 was irradiated with X-rays. A schematic of the set-up and the spectrum of the X-ray tube is shown in Fig. 5.2.
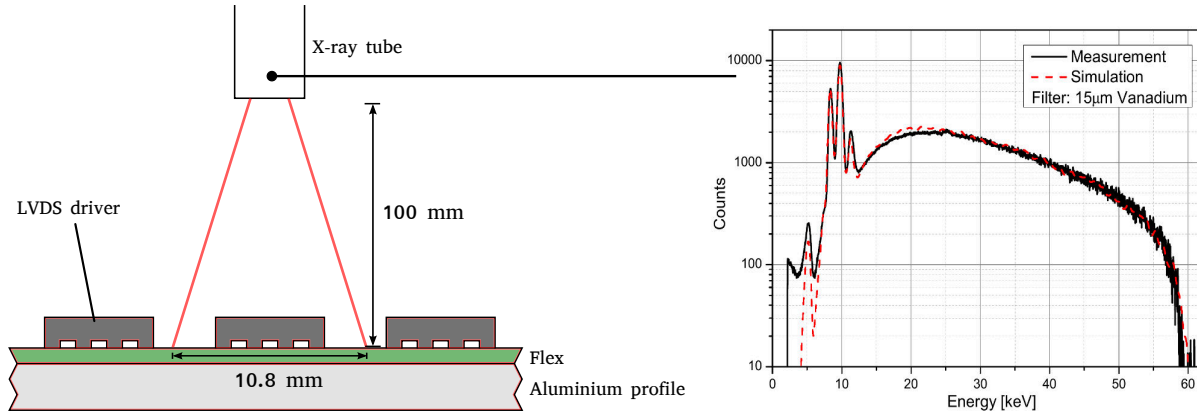
Figure 5.2: Set-up of the irradiation and the measured photon spectrum [42] after a 15 μm thick vanadium filter of the X-ray tube. The distance between the X-ray tube and LVDS driver is kept constant at 100 mm as well as the irradiated spot with a diameter of 10.8 mm for homogeneous irradiation of the IC.

The X-ray tube uses a vanadium filter and a supplied voltage of 60 kV to provide a comparable photon spectrum with the expected synchrotron radiation spectrum during the BEAST II experiment.

In addition to the investigated influence of the total dose, the effect of different dose rates from 74 krad/hour to 372 krad/hour on the internal CMOS is studied. The selected steps are listed in Tab. 5.1.

Irradiation time / h:min	Dose rate / krad/h	Integrated Dose / krad
0:33	186	100
0:49	186	250
1:20	186	500
1:40	298	1000
1:20	74	1100
1:47	223	1500
6:43	74	2000
1:04	186	2200
1:36	186	2500
2:41	186	3000
2:41	372	4000

Table 5.1: Irradiation steps with varying dose rates up to an integrated dose (TID) of 4 Mrad.

In order to mimic final irradiation conditions, the IC is operated regularly (bias voltage) and kept cold at 10 °C. Since annealing of the silicon oxide in the CMOS is temperature dependent, the cool down inhibits that process and allows measurements under realistic conditions.

In order to investigate the change in the current consumption, 2 V are applied to the LVDS driver, reading out the current consumption every 60 s from a source-meter.

For the period of irradiation, the current consumption shows the behaviour as it is shown in Fig. 5.3.
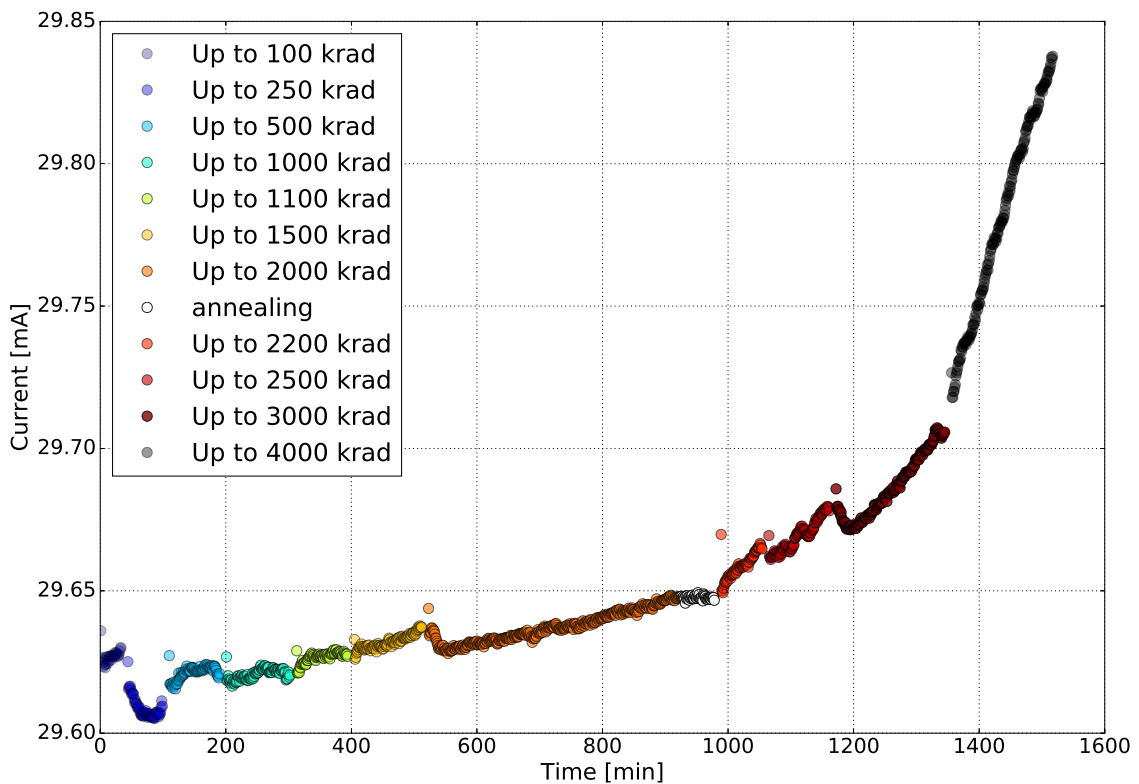
Figure 5.3: The current consumption of the LVDS drivers as a function of the radiation time. The color code shows the total achieved dose after each step using different dose rates. The current increase after a TID of 4 Mrad is 1 %.

The effect of the radiation dose on the internal transistor is visible: The higher the integrated dose, the higher the current consumption. The current drops in the first 200 minutes of irradiation which can be explained by the different behaviour of the CMOS transistor consisting of an NMOS and PMOS. Both can react differently and therefore the prediction of the precise origin of the current change is challenging. After roughly 900 minutes, for a short period of time annealing takes place. This means that the detector is operated but not irradiated and the current remains stable, marked as white dots in the diagram.

The measurement shows that the irradiation of the LVDS driver to an integrated dose of 4 Mrad

results in an increase of 0.2 mA in the current consumption. This is an increase of approximately 1 %. The slight increase will have no significant impact on the experiment.

In order to investigate the influence of the radiation damage on the signal integrity of the HitOr signal, an oscilloscope is used to measure the waveform of the signal at the Intermediate flex and after 28 m of propagation and patch panel at the readout board. For this reason, a calibration pulse of 280 PlsrDAC is injected in 200 pixels of the FE-I4, using the internal charge injection. The waveform of the signals is displayed and shown in Fig. 5.4 for an unirradiated state and after a TID of 4 Mrad.
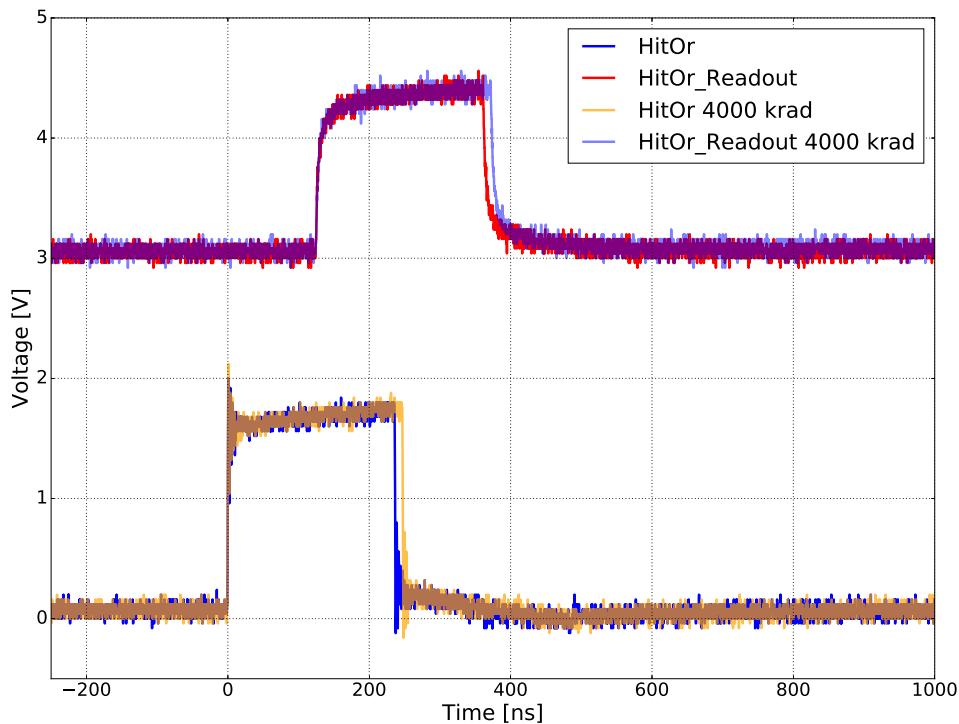
Figure 5.4: The diagram of the waveforms showing the HitOr signal before and after irradiation at the position of the Intermediate flex and at the back-end electronics. Each signal at the readout board has a manually induced offset of 3.0 V for better visualization.

The diagram shows that the irradiation up to the maximum dose has no impact on the transmission quality of the signal. After 28 m of propagation, the recorded signal shows no variation. This is in good agreement with the observed current increase of 1 %.

The reason for a slightly wider signal of the HitOr after the irradiation is due to differences in the PlsrDAC injection because of the discussed transistor mismatches. It can be the case that different pixels were taken in the oscilloscope measurement before and after the irradiation. Consequently, the radiation dose of 4 Mrad has no major influence on the performance of the LVDS driver.

Thermal tests

In this chapter, the working principle of the supported cooling for the FANGS staves is described in depth, since it is the first prove of the installation. In addition, measurements are carried out, using a thermal camera to investigate the temperature distribution of a fully powered stave.

6.1 Cooling concept

A single FANGS module consists of five FE-I4 glued on an aluminium stave. In parallel operation, all FE are biased ($V_{\text{Bias}} = 2\,\text{V}$), resulting in a current consumption of about $600\,\text{mA}$ per FE-I4. In total, this yields to a power consumption for the whole module of $P_{\text{total}} = U \cdot I = 6\,\text{W}$. With an chip area of $3.88\,\text{cm}^2$, it results in a power density of $0.309\,\text{W/cm}^2$ in total.

In order to cool down the electronics and sensors, FANGS modules are attached to the implemented cooling system of the PXD: the support and cooling block (SCB), as shown in Fig. 6.1.
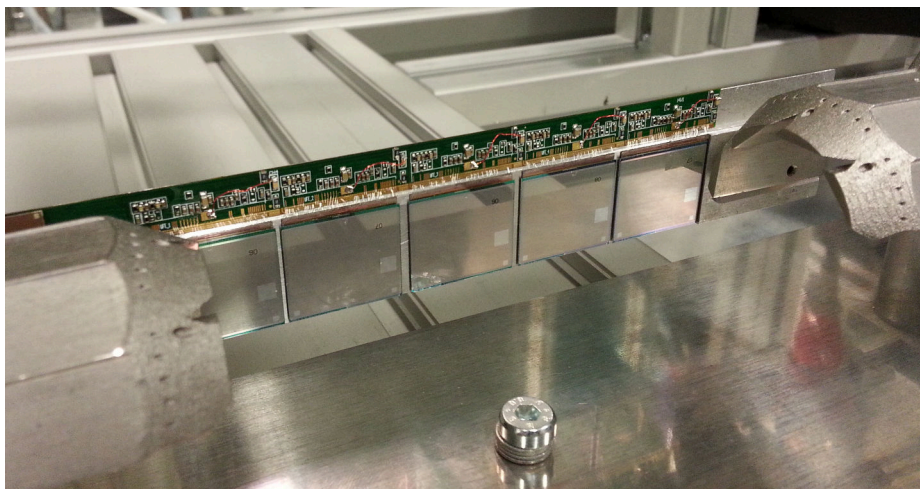
Figure 6.1: Integration of a FANGS stave on the support and cooling block (SCB) of the PXD. The stave is mounted with screws, using the prepared holes in the SCB and the aluminium profile.

The cooling mechanism through the SCBs should ensure a homogeneous and sufficiently low temperature distribution which is required to have proper operational conditions for the FE-I4 sensors. At DESY[1] in Hamburg, a reproduction of the SCBs is located [43], giving the opportunity to check the integration of the stave and verify the cooling concept for FANGS.
The two SCBs are made of stainless steel which are assembled in two half shells and have the same mechanical and thermal properties as in the final experiment.
The chosen cooling technology is a two-phase carbon dioxide (CO_2) cooling in combination with nitrogen (N_2) air flow. As illustrated in Fig. 6.2, integrated cooling channels are implemented within the SCB.
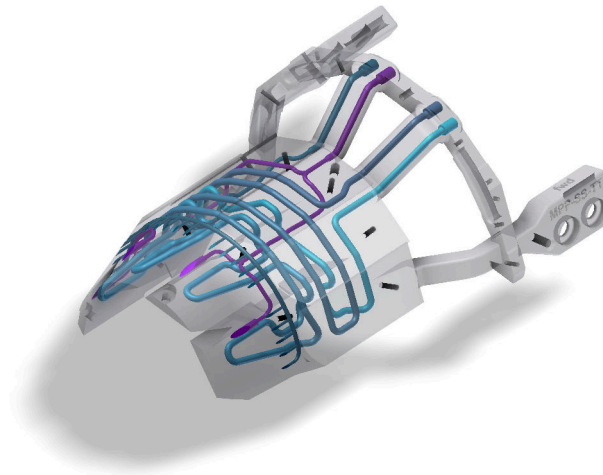
Figure 6.2: The design of the SCB. The integrated channels for CO_2 circulation and N_2 air flow are within the SCB profile [43].

The two-phase transition enables the heat dissipation by evaporating liquid CO_2 in closed channels. In addition, open channels are included for the N_2 air flow along the FANGS staves, reducing the humidity and thus preventing condensation and ice formation on sensors of the FE and the SCBs as well.

6.2 Temperature measurements

The set-up is mounted in a sealed box to avoid any gas exchange with the environment. The open channels provide the injection of N_2 at room temperature, ensuring a low humidity and constant temperature in the box. The SCB temperature is set to -10 °C with a constant CO_2 pressure controlled by a cooling plant based on an accumulator [44]. The modules are fixed with two screws at the SCBs. One elongated hole allows possible movement of the aluminium profile due to CTE mismatches.
The measurements are performed with a thermal camera attached to the front side of the box and temperature probes for control and calibration on the back. The measurement procedure is divided into two parts: At first, the temperature distribution of one FANGS stave in idle state is

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[1] Deutsches Elektronen-Synchrotron

observed and afterwards, the five FE and sensors are powered and the temperature profile, due to heat dissipation, is measured. In Fig. 6.3, the recorded data of the thermal camera is plotted in heat maps.
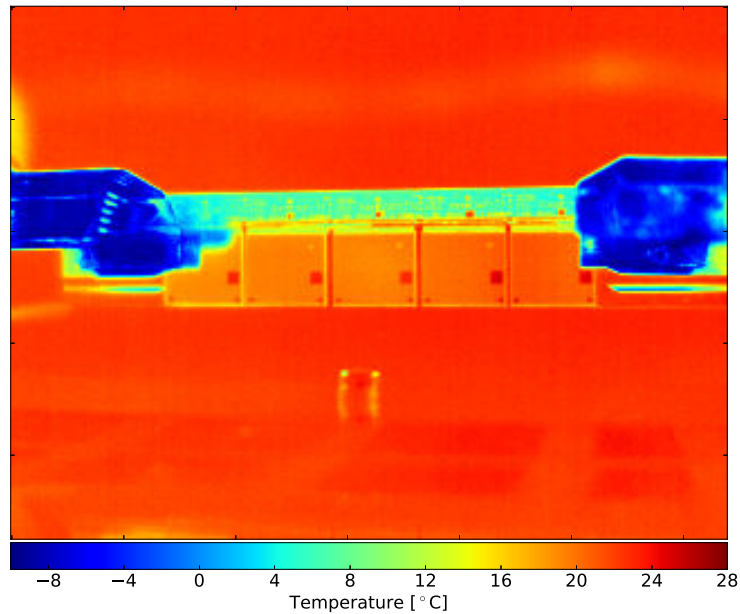
(a) Heat map with FANGS in idle state.
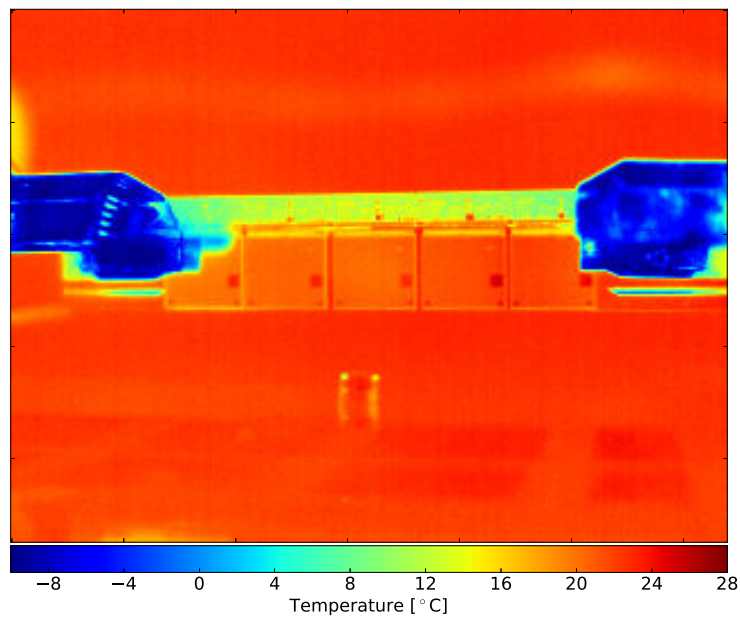
(b) Heat map with nominal running conditions in the detector (bias voltages and HV).

Figure 6.3: Thermal images showing a FANGS module attached to the SCBs at both ends. The central region with five FE-I4 is visible. The temperature of the SCBs is in both images $T_{\text{SCB}} = -9\,^\circ\text{C}$.

For both heat maps, a temperature of -9 °C on the surface of the SCB can be observed. When considering the temperature of the flex without power supplied FE, a gradient temperature distribution is observable, recording a temperature of 10 °C on the center part of the flex. After powering up, a shift of the temperature occurs. Because of the heat load the temperature of the FE is increased up to 25 °C. Due to reflections on the sensor surface, which can be seen on the first chip on the left, this value is an approximation of the real temperature of the FE.

In order to have a better overview of the temperature change, the difference between the heat maps is depicted in Fig. 6.4. Changes in the temperature of the environment and the SCB surface are not observable. The highest change is observed on the flex with a maximum temperature increase of 6.5 °C with respect to the starting state conditions.
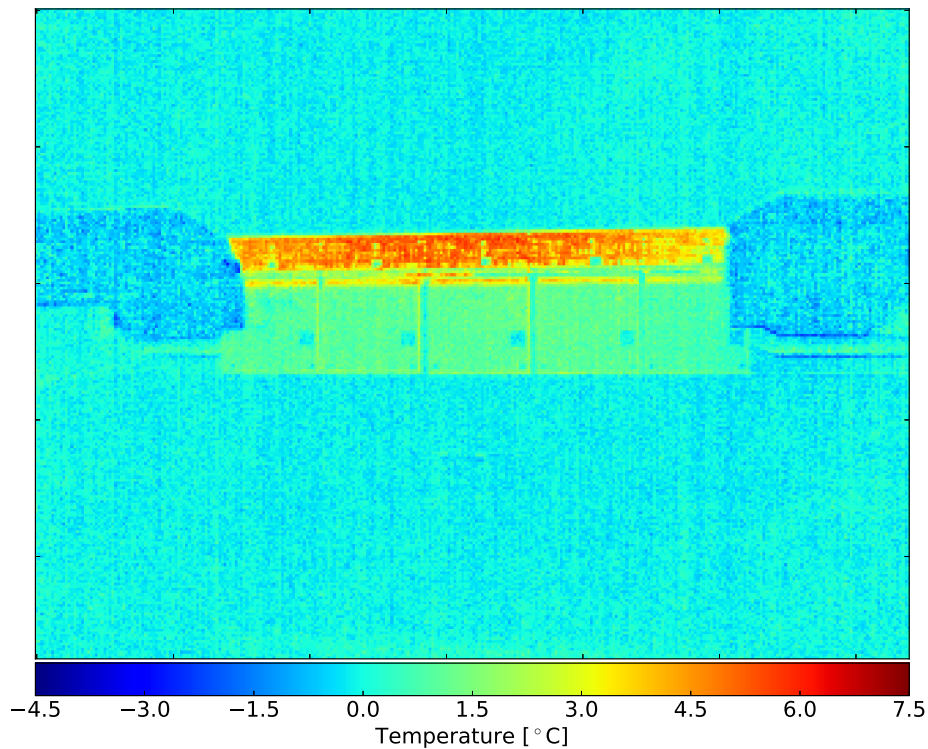
Figure 6.4: Difference between the thermal images in Fig. 6.3, showing the temperature change after powering the five FE-I4 and sensors.

In order to further investigate the behaviour of dissipated heat, Pt100[1] sensors are used to measure the temperature increase at different positions of the set-up.

The sensor is placed in three positions: On the surface of the SCB, on the backside of the aluminium profile and in the environment without support. The measured values are shown in Tab. 6.1.

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[1] Platinum temperature sensor, using the change of resistance in the metal caused by temperature changes.

	Without heat load	With heat load
SCB	$-9.8\,°C$	$-10.0\,°C$
Profile	$7.0\,°C$	$12.5\,°C$
Environment	$16.0\,°C$	$19.5\,°C$

Table 6.1: Temperature measurements with three Pt100 at different positions. The measurement uncertainty is $0.1\,°C$.

The CO_2 flow causes a temperature of $-10\,°C$ at the surface of the SCBs, which is in good agreement with the recorded values of the thermal camera. The dissipated heat implements an increase of $5.5\,°C$ on the backside of the profile as well as in the environment. Since there is a shielding of 2 mm aluminum between the FE and the Pt100, the exact temperature of the electronics and sensors cannot be determined.

However, the measurement qualitatively shows that the operating temperature range of the FE-I4 from $-40\,°C$ to $60\,°C$ (given in Tab. 1.1) is not exceeded under realistic conditions.

6.3 Temperature control in the experiment

In the BEAST II experiment, the temperature distribution along each FANGS stave will be measured using optical sensors from `Smart Fibres` [45]. The technology is based on fibre Bragg gratings (FBG) which are placed in optical fibres. This technique uses periodic variations of the refractive index in the fibre, the so-called FBG region. If a broad-spectrum of light is emitted and enters the fibre, reflections occur at the FBG region, which interfere constructively at the Bragg wavelength. The FBG reflects the Bragg wavelength of light while transmitting all others, as it is shown in Fig. 6.5.
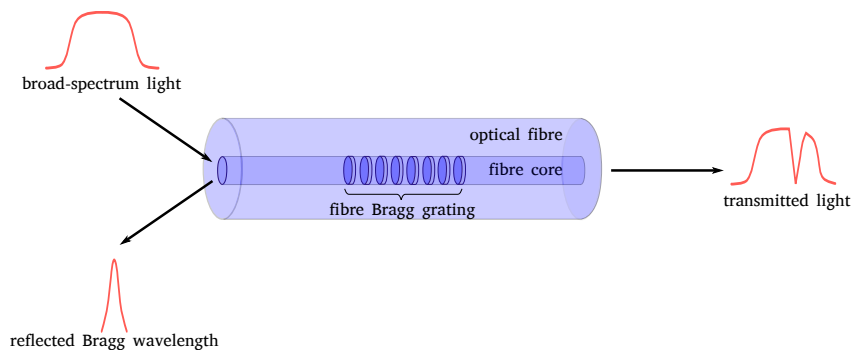
Figure 6.5: Sketch of the working principle of FBG optical sensor showing the transmitted and reflected spectrum. The reflected Bragg wavelength is measured.

Slight changes in the temperature and strain on the fibres affect a shift of the Bragg wavelength. To be sensitive to temperature changes, the FBG must remain unstrained so that the FBG reflects a wavelength of light that shifts in response to temperature variations. For a temperature range

of -30 °C to 60 °C, the measured Bragg wavelength can be converted to the related temperature. In the experiment, the system will be implemented in a small 1×1 mm^2 gap milled on the backside of the aluminium profile of FANGS. In Fig. 6.6, the FBG fibre on the backside of the profile is photographed.
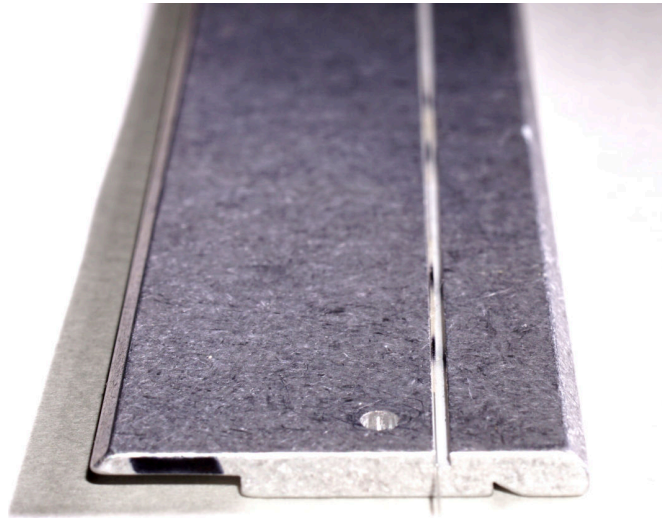
Figure 6.6: A picture of the backside of the aluminium profile showing the 1×1 mm^2 gap where the FBG is inserted. The black regions along the fibre are the implemented FBG regions.

Since the FBG fibre is on the backside of the stave, it provides the temperature measurement due to the heat of the five FE-I4 into the aluminium profile with 2 mm aluminium separating both components. In the experiment, the temperature will be measured in five different points along the stave.

Integration of BEAST II

In the final chapter, the integration of the BEAST II sub-detectors into the VXD volume is discussed. The physical sizes and attachment points of the sub-detectors are limited by the volume and support structure. The existing PXD infrastructure, in particular the SCBs, is used as a support for FANGS. The mounting sequences of the system integration are listed and described according to their order:

- The starting point of the mounting sequence is the beryllium beam pipe with an inner gold plating, shown in Fig. 7.1(a). Diamond sensors are installed giving information about the instantaneous and accumulated radiation. They are connected to the beam abort, the so-called interlock system, to stop the beams if radiation is higher than tolerated.

- After mounting the SCB, two layers of the final PXD are installed. This part of the detector will be installed in the Belle II detector, using the same mechanical configuration. They are mounted at 0° in ϕ direction. The set-up is depicted in Fig. 7.1(b).

- Figure 7.1(c) shows the following sequence in which three FANGS staves are mounted with screws on the two SCBs. Located at the distance of the second PXD layer, they are covering 90°, 180° and 270° in ϕ. The three Intermediate flexes are located in the backward region of the detector.

- Subsequently, CLAWS and PLUME are added to the volume, shown in Fig. 7.1(d). Both are located at 155° and 225° in ϕ.

- The final step of the integration includes the installation of four layers of the final SVD. Placed at 0° behind the PXD there is the SVD cartridge, shown in Fig. 7.2.

The cable routing will be carried out over dock boxes in the backward region of the VXD volume where the service connections of all sub-detectors will be located. In this place, the patch panel will be positioned. The DAQ systems will be in a moveable building next to the detector, referred to as electronics hut. Separated into rack spaces, it provides enough space to store readout electronics and power supply for all detector types.

(a) Beam pipe and diamond sensors.

(b) SCB and PXD installation.

(c) FANGS.

(d) CLAWS and PLUME.
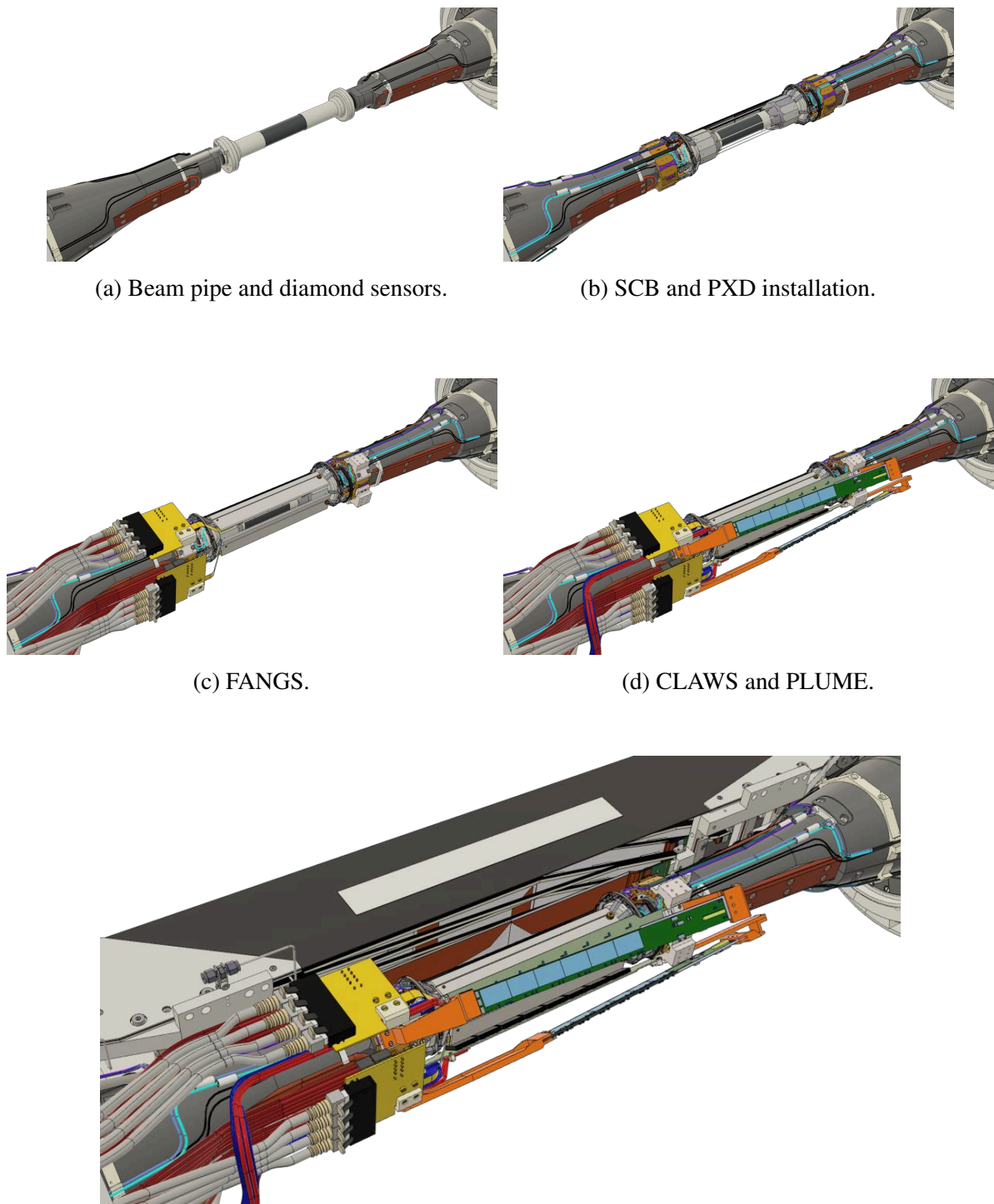
Figure 7.2: The final layout of the BEAST II experiments including all installed sub-detectors and the supporting structure of the VXD volume [25].

The received data from the FANGS detector will be streamed to the SuperKEKB accelerator control room since it will be a key ingredient for the machine commissioning.

Conclusion and Outlook

The presented work focusses on the development of the FANGS detector which will be installed in the BEAST II experiment at the SuperKEKB accelerator. The experiment will help in the SuperKEKB machine commissioning and ensure background safe conditions for the VXD installation.

In the framework of this thesis, the detector system and readout electronics were connected and tested for the first time, using a set-up with final cable lengths and components. The sophisticated DAQ system, i.e. the new readout board (MMC3), was checked. As a result, the TDC module was embedded in the firmware of the FPGA enabling the fast charge sampling capability of the 640 MHz clock provided by the FPGA.

Several measurements were carried out with five FE-I4 located on the FANGS stave and pointed out the functionality of the FE-I4-based module and the charge collection in the sensor. In order to achieve precise energy information about the background radiation, the charge calibration of each FE-I4 used in the experiment is mandatory. The first FANGS stave was therefore assembled and fully characterized.

In addition, the thesis presented the resistance of the data transmission driver exposed to X-rays in the range of expected synchrotron radiation and total ionizing dose during the experiment. After irradiation, signal quality was maintained and the performance has been validated in a realistic environment.

The FANGS cooling concept uses the support and cooling blocks of the PXD, and therefore the evaluation of the integration of the stave was carried out. In addition, the capability of heat dissipation in the layout was studied. The results showed that the maximum tolerable temperature of the FE-I4 was not exceeded with nominal running conditions.

Finally, the BEAST II mounting sequences were presented including the three FANGS staves with a total amount of fifteen FE-I4 readout chips based on the ATLAS IBL pixel detector modules.

Outlook

The promising results about the development and test phase of the FANGS detector presented in this thesis can be regarded as a motivation for some further research before the commissioning

of the detector in the BEAST II experiment in mid-term of 2017. This can include a full performance test of all three staves at the same time under realistic conditions as well as the real time monitoring of incoming data.

Finalized tests are feasible at a test beam campaign. The performance test requires additional scripts and algorithms reacting to possible errors which can also occur in the final experiment. Another aspect concerns the synchronization of the individual detectors of the experiment, providing measurements depending on time and position. Various trigger methods, e.g. trigger on a certain frequency or the injection of particle bunches have to be discussed and thus implemented in the FANGS system.

The availability and functionality of all components accomplished in the work of this thesis, i.e. the FANGS stave and the DAQ system, allow to reach the goal of radiation monitoring with FANGS in the BEAST II experiment.

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PlsrDAC calibration

This chapter contains the additional recorded energy spectra and PlsrDAC calibrations for each FE-I4 on the FANGS stave. The slope and offset from the PlsrDAC calibration can be used to convert from PlsrDAC to keV in the BEAST II experiment.

A.1 Chip 2
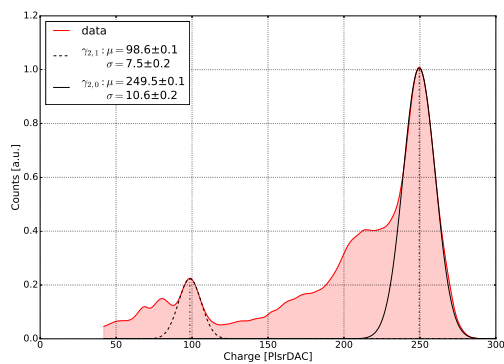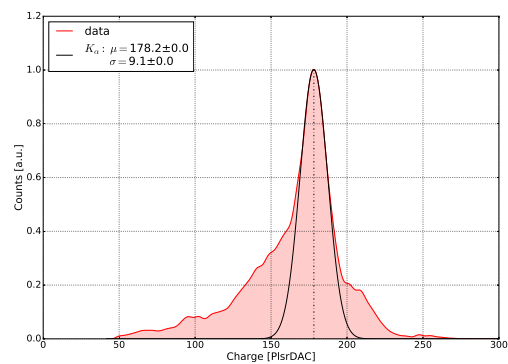
(a)   (b)
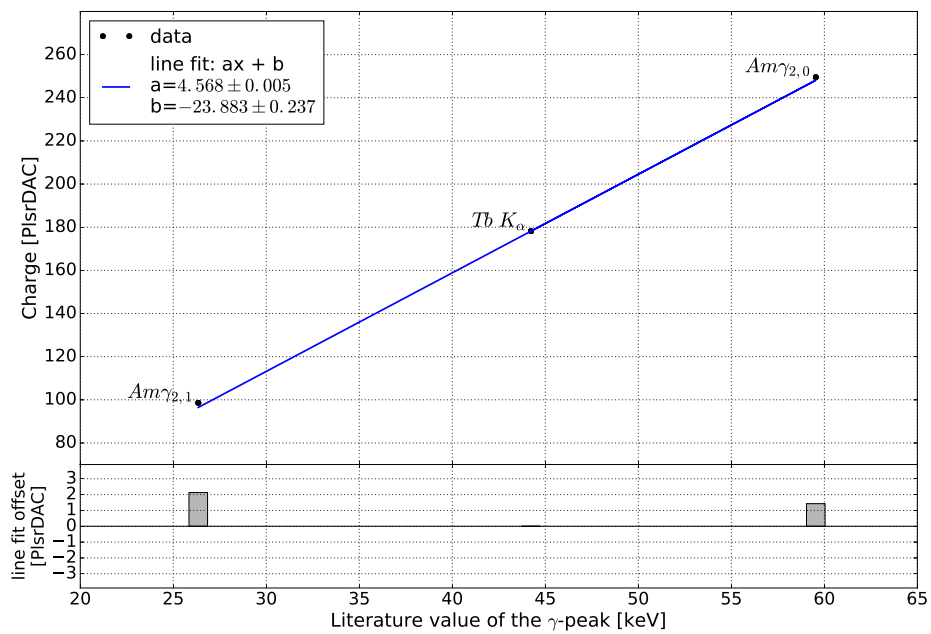
Figure A.2: PlsrDAC calibration using the extracted peak values from the source scans. Recorded spectra of ^{241}Am (a) and ^{56}Tb (b). The bars in the lower part indicate the distance of the value to the line fit.

A.2 Chip 3

(a)

(b)
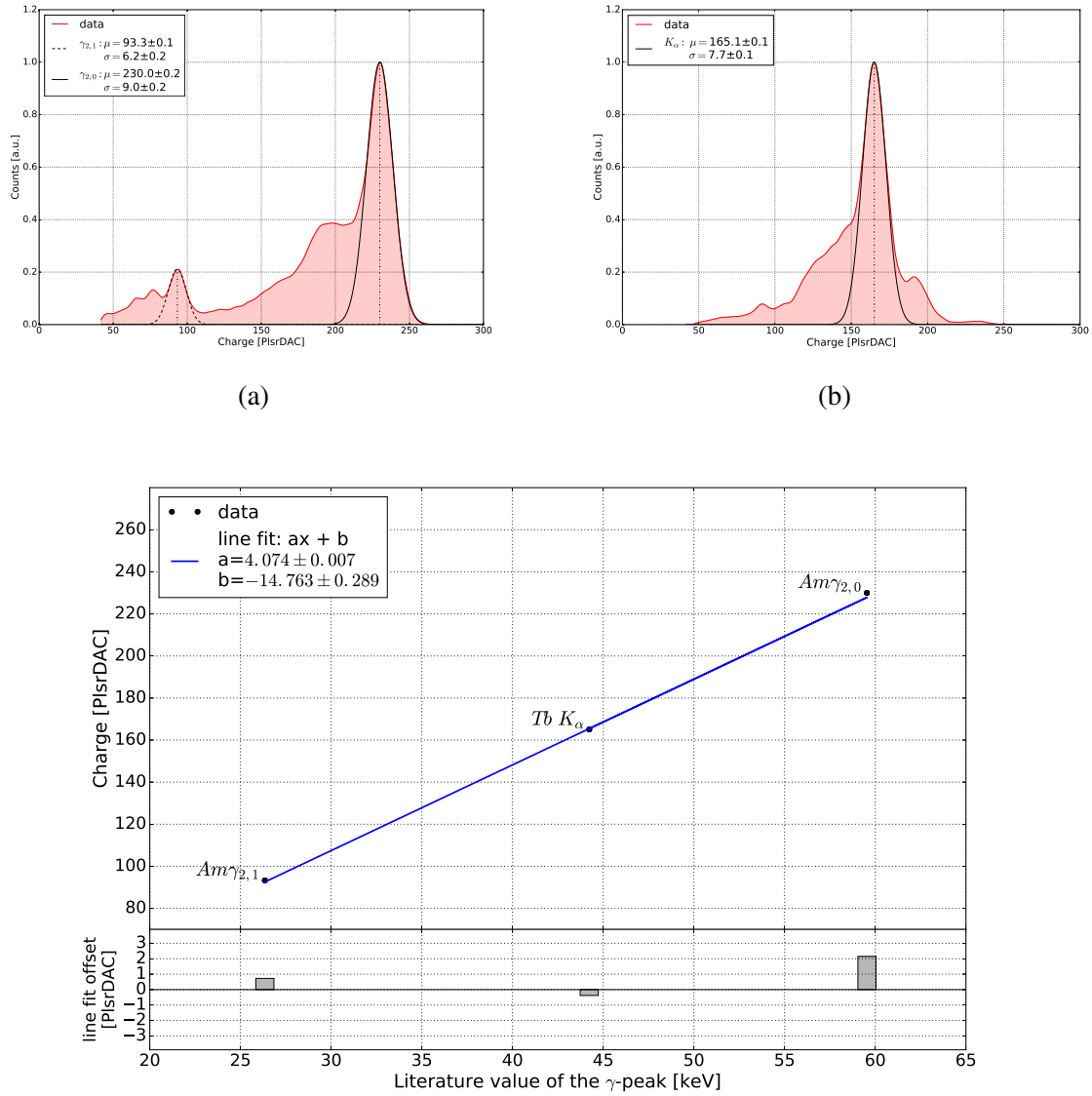
Figure A.3: PlsrDAC calibration using the extracted peak values from the source scans. Recorded spectra of ^{241}Am (a) and ^{56}Tb (b). The bars in the lower part indicate the distance of the value to the line fit.

A.3 Chip 4

(a)   (b)
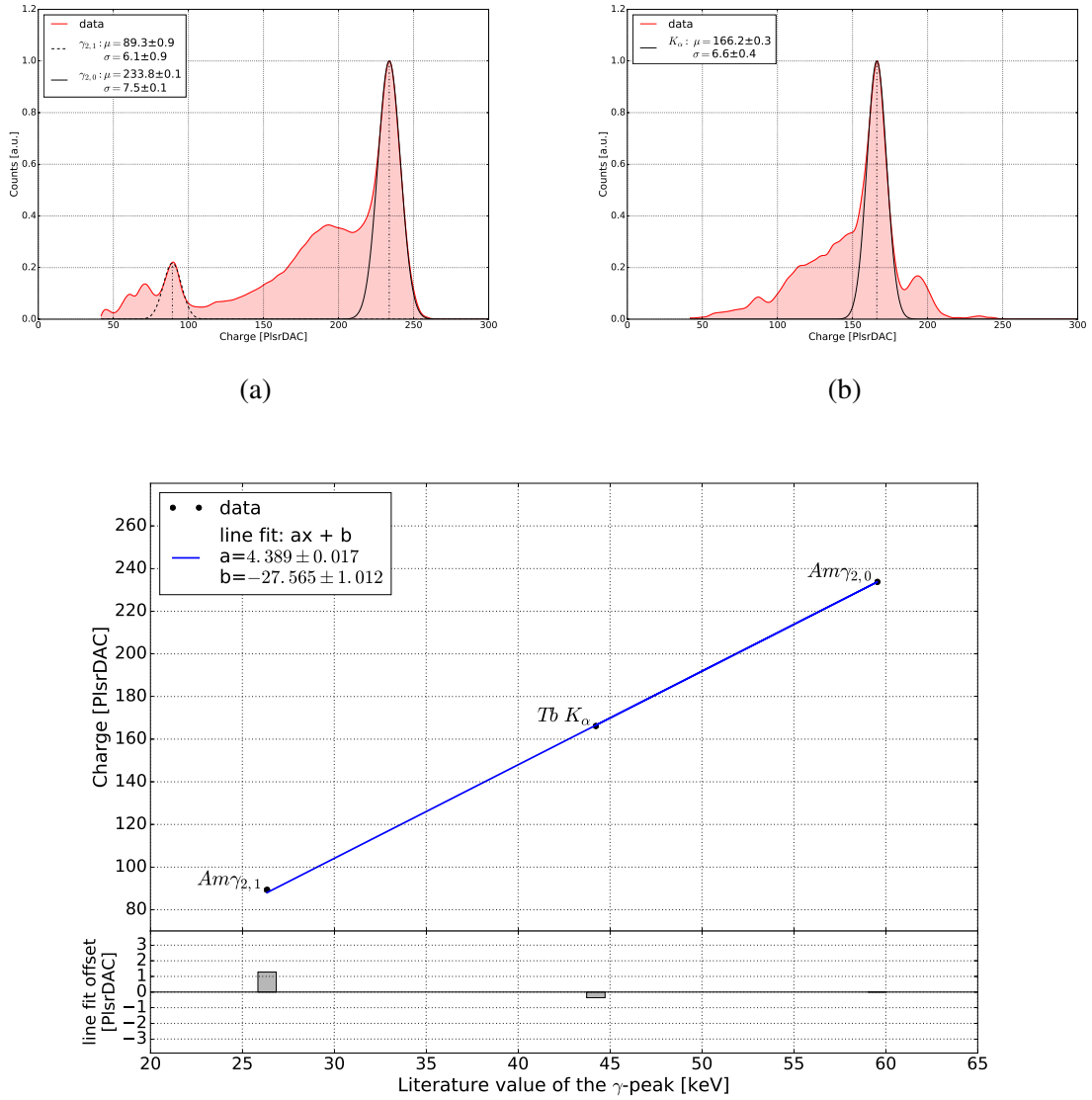
Figure A.4: PlsrDAC calibration using the extracted peak values from the source scans. Recorded spectra of ^{241}Am (a) and ^{56}Tb (b). The bars in the lower part indicate the distance of the value to the line fit.

A.4 Chip 5

(a)

(b)
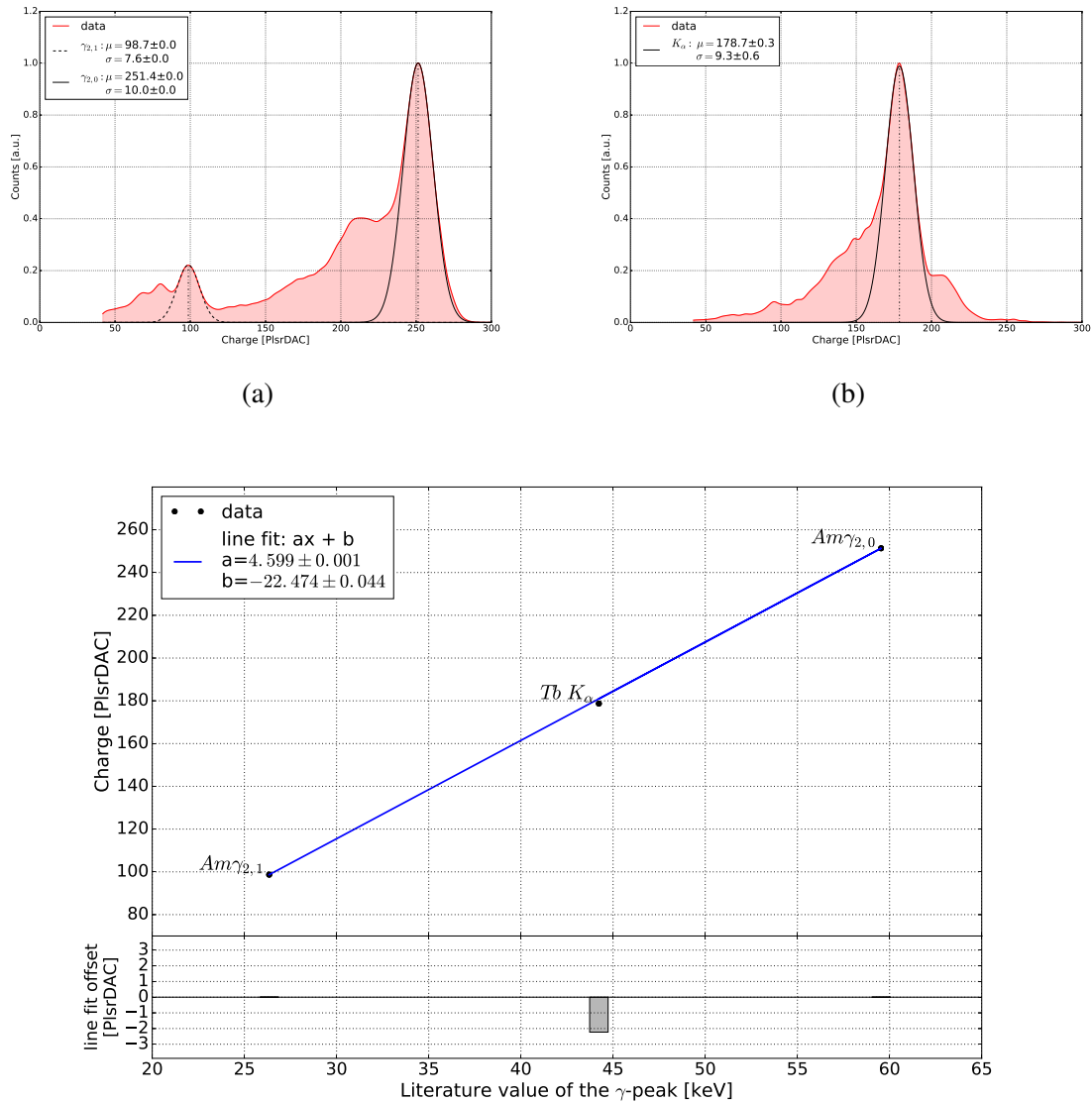
Figure A.5: PlsrDAC calibration using the extracted peak values from the source scans. Recorded spectra of ^{241}Am (a) and ^{56}Tb (b). The bars in the lower part indicate the distance of the value to the line fit.

List of Acronyms

ARICH   Aerogel Ring Cherenkov detector

BEAST   Beam Exorcism for A Stable Experiment

CDC   Central Drift Chamber

CLAWS   sCintillation Light And Waveform Sensors

CLK   clock

CMD   command

CMOS   Complementary Metal-Oxide-Semiconductor

CSA   charge-sensitive amplifier

CTE   Coefficient of Thermal Expansion

DAC   Digital-to-Analog Converter

DAQ   data acquisition

DEPFET   Depleted P-Channel Field Effect Transistor

DESY   Deutsches Elektronen-Synchrotron

DSSD   Double Sided Silicon Strip Detector

ECL   Electromagnetic calorimeter

FANGS   FE-I4 ATLAS Near Gamma Sensor

FBG   fibre Bragg grating

FE   Front-End

FPGA   Field-Programmable Gate Array

HDL   Hardware Description Language

HER   High Energy Ring

HV	High Voltage
IBL	Insertable B-Layer
IC	integrated circuit
ID	identification
IR	interaction region
JTAG	Joint Test Action Group
KIT	Karlsruhe Institute of Technology
KLM	K_L and muon detector
LDO	low drop-out regulator
LER	Low Energy Ring
LHC	Large Hadron Collider
LVDS	low-voltage differential signalling
MIO	Multi Input / Output
MMC3	Multi Module Card 3
PCB	printed circuit board
PID	Particle identification system
PLUME	Pixelated Ladder using Ultra-light Material Embedding
PS	power supply
PXD	Pixel Detector
QCS	Quadrupole and Compensation Solenoids
RPC	Resistive Plate Counter
SCB	support and cooling block
SiPM	silicon photomultiplier
SM	Standard Model
SVD	Silicon Vertex Detector
TDC	Time-Digital-Converter

TID	total ionizing dose
TOP	Time-Of-Propagation detector
ToT	Time-over-Threshold

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Acknowledgements